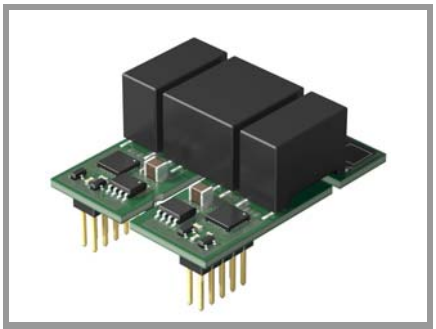
SKYPER 12 PV R



SKYPER®

Driver Core

Order Number
L5070901

Datasheet valid for L5070901 Index 01

SKYPER 12 PV R

Features*

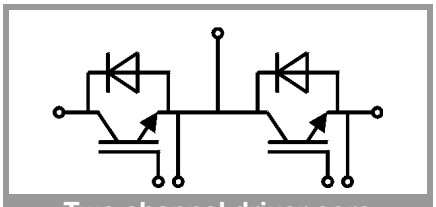
- Two output channels
- Integrated power supply
- Selectable dead time
- Dynamic short-circuit protection
- SoftOff in case of secondary side error
- Selectable filter setting
- Multi failure management
- RoHS, UL recognized
- Coated with SL1307

Typical Applications

- Driver for IGBT modules in bridge circuits in industrial application

Remarks

- The insulation test is not performed as 100% series test at SEMIKRON
- The maximum DC-link voltage is limited by the creepage and clearance distances; according to EN 62109-1, PD II, OVC III & EN 61800-5-1, PD II, OVC III
- Operating temperature is real ambient temperature around the driver core
- Environmental conditions are stated in Technical Explanation



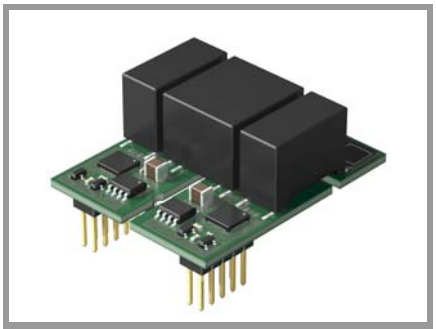
Two channel driver core

Absolute Maximum Ratings

Symbol	Conditions	Values	Unit
V_s	Supply voltage primary side	15.5	V
V_{IH}	Input signal voltage (HIGH)	Vs + 0.3	V
V_{IL}	Input signal voltage (LOW)	GND - 0.3	V
$I_{out(peak)}$	Output peak current[1)]	20	A
$I_{out(avg)}$	Output average current[1)]	50	mA
f_{max}	Maximum switching frequency[2)]	100	kHz
V_{CE}	Collector emitter voltage[3)]	1700	V
V_{DC}	DC-Link voltage[4)]	1500	V
dv/dt	Rate of rise and fall of voltage secondary to primary side	50	kV/µs
V_{isol}	Insulation test voltage input-output (AC, rms, 2s)[5)]	5000	V
Q_{out}	Output charge per pulse[6)]	20	µC
T_{op}	Operating temperature range	-40 ... 85	°C
T_{stg}	Storage temperature range	-40 ... 85	°C

Characteristics

Symbol	Conditions	min.	typ.	max.	Unit
V_s	Supply voltage primary side	14.55	15	15.45	V
$V_{UVLO(prim)}$	Primary side undervoltage-lockout shutdown threshold	12.2			V
	Primary side undervoltage-lockout reset threshold			13.9	V
$V_{UVLO(secP)}$	Secondary side undervoltage-lockout shutdown threshold, positive gate voltage	9.4			V
	Secondary side undervoltage-lockout reset threshold, positive gate voltage			13.3	V
$V_{UVLO(secN)}$	Secondary side undervoltage-lockout shutdown threshold, negative gate voltage			-4.1	V
	Secondary side undervoltage-lockout reset threshold, negative gate voltage	-5.8			V
$I_{S(idle)}$	Supply current primary side (no load)		110		mA
$I_{S(max)}$	Supply current primary side (full load)			400	mA
V_I	Input signal voltage on/off		Vs/0		V
V_{IT+}	Input threshold voltage (HIGH)	11			V
V_{IT-}	Input threshold voltage (LOW)			4	V
$R_{IN(sw)}$	Input resistance (switching signals)		33		kΩ
$C_{IN(sw)}$	Input capacitance (switching signals)			0.01	nF
$V_{G(on)}$	Turn-on output voltage	15.1	15.4	15.8	V
$V_{G(off)}$	Turn-off output voltage		-9.5		V
$t_{d(on,ana)}$	Turn-on propagation delay time for analog filter selection		0.5		µs
$t_{d(on,dig)}$	Turn-on propagation delay time for digital filter selection		0.83		µs
$t_{d(off,ana)}$	Turn-off propagation delay time for analog filter selection		0.5		µs
$t_{d(off,dig)}$	Turn-off propagation delay time for digital filter selection		0.83		µs
$R_{IN(err,prim)}$	Input resistance (error input, primary side)		150		kΩ
$C_{IN(err,prim)}$	Input capacitance (error input, primary side)		10		nF



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- Dynamic short-circuit protection
- SoftOff in case of secondary side error
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Typical Applications

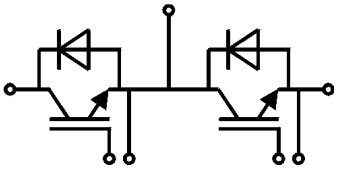
- Driver for IGBT modules in bridge circuits in industrial application

Remarks

- The insulation test is not performed as 100% series test at SEMIKRON
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- Operating temperature is real ambient temperature around the driver core
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Characteristics

Symbol	Conditions	min.	typ.	max.	Unit
$R_{IN(err,sec)}$	Input resistance (error inputs, secondary side)		150		kΩ
$C_{IN(err,sec)}$	Input capacitance (error inputs, secondary side)			0.01	nF
$t_{d(err)}$	Error propagation delay time[7)]		0.7		µs
$t_{d(err,ext)}$	External error propagation delay time[8)]		0.6		µs
t_{IDT}	Interlock dead time[9)]		2		µs
$t_{jitter(ana)}$	Signal transfer deviation for analog filter selection[10)]		± 3		ns
$t_{jitter(dig)}$	Signal transfer deviation for digital filter selection[10)]		± 12.5		ns
$t_{SPS(ana)}$	Short pulse suppression for analog filter selection		0.2		µs
$t_{SPS(dig)}$	Short pulse suppression for digital filter selection		0.39		µs
t_{POR}	Power-on reset time		0.15		s
t_{reset}	Error reset time[11)]	0.03			ms
$V_{CE(ref)}$	Reference voltage for V_{CE}-monitoring[12)]			9	V
$V_{ITH(clamp)}$	Input threshold voltage clamping (HIGH)[13)]			13	V
$V_{ITL(clamp)}$	Input threshold voltage clamping (LOW)[13)]	2			V
$R_{IN(clamp)}$	Input resistance (clamping inputs)		150		kΩ
$C_{IN(clamp)}$	Input capacitance (clamping inputs)			0.01	nF
$l_{clear(PS)}$	Shortest distance in air, primary side to secondary side	14			mm
$l_{clear(SS)}$	Shortest distance in air, secondary sides	6.1			mm
$l_{creep(PS)}$	Shortest distance along the surface, primary side to secondary side (CTI ≥ 400)	20.9			mm
$l_{creep(SS)}$	Shortest distance along the surface, secondary sides (CTI ≥ 400)	10.5			mm
V_{imp}	Impulse withstand voltage[14)]	12000			V
V_{PDPS}	Partial discharge extinction voltage, primary side to secondary side[15)]	2560			V
w	Weight		20		g
MTBF	Mean Time Between Failure[16)]		12		10^6h



Two channel driver core

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Footnotes

Footnote	Description
1)	The rated peak and average output current are valid over the full operating temperature range.
2)	The rated maximum switching frequency is valid for an operating temperature up to 75°C. For operating temperatures above 75°C the limits are specified according to the graph 'Maximum Switching Frequency'.
3)	Repetitive peak voltage across the semiconductor power rails.
4)	The maximum DC-Link voltage is limited by creepage and clearance distances (according to EN 62109-1, PD II, OVC III & EN 61800-5-1, PD II, OVC III).
5)	Test Conditions: ACrms, 2s, input to output
6)	If using power semiconductor modules with gate charges >1µC, the buffer capacitance of the driver's secondary sides and primary side has to be adjusted according to the corresponding Technical Explanation.
7)	Time between the driver detects an error at the secondary side until the primary side reports an error at the interface.
8)	Time between the driver receives an external error signal at the primary side until the driver turns off its outputs at the secondary side.
9)	The interlock dead time prevents the two outputs from being activated simultaneously. The dead time generation starts with each turn-off command at the driver's primary side. The interlock dead time generation could be deactivated via pin 'CFG_IDT'.
10)	The jitter is defined as the maximum deviation of the switching signal propagation delay time at constant environmental conditions. The signal transfer deviation $t_{jittter(ana)}$ is valid if analog filtering is selected via pin 'CFG_FLT' and the interlock dead time, generated by the controller, is longer than the interlock dead time which is ensured by the driver itself.
11)	Minimum time for which the driver is in error state.
12)	The driver detects a desaturation event, when one of its outputs is in on-state and the applied voltage at the corresponding V_{CE}-monitoring input (pin 'VCE_IN') exceeds the reference voltage for V_{CE}-monitoring. As long as the blanking time has not been elapsed, the desaturation detection is deactivated. The blanking time is adjustable via the 'CFG_VCE' pin.
13)	The driver's output switches to high-resistance state, when the output is in off-state and the applied voltage at the corresponding 'CLMP_IN' pin exceeds the input threshold voltage $V_{ITH(clamp)}$. The output returns to off-state when the applied voltage at pin 'CLMP_IN' falls below the input threshold voltage $V_{ITL(clamp)}$.
14)	Test condition: 12000V, pulse according to EN 62109-1 & EN 61800-5-1
15)	The partial discharge extinction voltage in this data sheet is defined as peak voltage.
16)	Conditions: T_{op} = 40°C; full load. Theoretical consideration according to SN 29500.
17)	All external circuits, except the V_{CE} reference voltage adjustment, have to be supplied via pin 'PWR_VS_P_OUT' with respect to pin 'PWR_VS_N_OUT'. The rated average output current is reduced by the supply current of these external circuits.

Pin description - primary side

PIN	Signal	Function	Specifications
X10:01	PWR_GND	Ground potential for power supply and digital signals	To be connected to ground
X10:02	CFG_IDT	Interlock dead time configuration	15V logic; 150kΩ (pull-up) LOW = 2µs interlock dead time HIGH = No interlock dead time
X10:03	nERR_OUT	Error output	Open collector output; max. 18V/15mA (external pull-up resistor needed) LOW = Error HIGH = No error
X10:04	nERR_IN	Error input	15V logic inverted; 150kΩ/10nF (pull-up) LOW = External error HIGH = No external error
X10:05	CFG_ERR	Error behavior configuration in case of secondary side error	15V logic; 150kΩ (pull-down) LOW = Both outputs switch off HIGH = Affected output switches off
X10:06	CFG_FLT	Filter configuration for switching signals	15V logic; 150kΩ (pull-down) LOW = Analog filter ($t_{SPS(ana)}$) HIGH = Digital filter ($t_{SPS(dig)}$)
X10:07	TOP_IN	Switching signal input (TOP)	15V logic; 33kΩ/0.01nF (pull-down) LOW = TOP switch off HIGH = TOP switch on
X10:08	BOT_IN	Switching signal input (BOT)	15V logic; 33kΩ/0.01nF (pull-down) LOW = BOT switch off HIGH = BOT switch on
X10:09	PWR_VS	Driver power supply	Stabilized +15V ±3%
X10:10	PWR_VS	Driver power supply	Stabilized +15V ±3%

Pin description - secondary side - TOP

PIN	Signal	Function	Specifications
X100:01	CFG_VCE	V_{CE}-monitoring reference voltage	External voltage divider needed
X100:02	VCE_IN	V_{CE}-monitoring input	External blocking diode needed
X100:03	PWR_VS_P_OUT	Power supply output, positive voltage	Equal to $V_{G(on)}$ [17)] (external buffer capacitors can be connected)
X100:04	nERR_IN	External error input	15V logic inverted; 150kΩ/0.01nF (pull-up) LOW = External error HIGH = No external error
X100:05	TOP_ON	On signal path to TOP semiconductor	External gate resistor needed (in consideration of $I_{out(avg)}$, $I_{out(peak)}$, $V_{G(on)}$)
X100:06	TOP_OFF	Off signal path to TOP semiconductor	External gate resistor needed (in consideration of $-I_{out(avg)}$, $-I_{out(peak)}$, $V_{G(off)}$)
X100:07	CLMP_IN	V_{CE}-clamping input	150kΩ/0.01nF (pull-down) In case of activated TOP_OFF: LOW = TOP_OFF equal to $V_{G(off)}$ HIGH = TOP_OFF floating
X100:08	PWR_GND	Ground potential for power supply and digital signals	Reference potential for gate voltages (emitter/source of power semiconductor)
X100:09	TOP_SOFTOFF	SoftOff signal path to TOP semiconductor	External gate resistor needed
X100:10	PWR_VS_N_OUT	Power supply output, negative voltage	Equal to $V_{G(off)}$ [17)] (external buffer capacitors can be connected)

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Pin description - secondary side - BOT

PIN	Signal	Function	Specifications
X200:01	CFG_VCE	V_{CE}-monitoring reference voltage	External voltage divider needed
X200:02	VCE_IN	V_{CE}-monitoring input	External blocking diode needed
X200:03	PWR_VS_P_OUT	Power supply output, positive voltage	Equal to $V_{G(on)}$ [17)] (external buffer capacitors can be connected)
X200:04	nERR_IN	External error input	15V logic inverted; 150kΩ/0.01nF (pull-up) LOW = External error HIGH = No external error
X200:05	BOT_ON	On signal path to BOT semiconductor	External gate resistor needed (in consideration of $I_{out(avg)}$, $I_{out(peak)}$, $V_{G(on)}$)
X200:06	BOT_OFF	Off signal path to BOT semiconductor	External gate resistor needed (in consideration of $-I_{out(avg)}$, $-I_{out(peak)}$, $V_{G(off)}$)
X200:07	CLMP_IN	V_{CE}-clamping input	150kΩ/0.01nF (pull-down) In case of activated BOT_OFF: LOW = BOT_OFF equal to $V_{G(off)}$ HIGH = BOT_OFF floating
X200:08	PWR_GND	Ground potential for power supply and digital signals	Reference potential for gate voltages (emitter/source of power semiconductor)
X200:09	BOT_SOFTOFF	SoftOff signal path to BOT semiconductor	External gate resistor needed
X200:10	PWR_VS_N_OUT	Power supply output, negative voltage	Equal to $V_{G(off)}$ [17)] (external buffer capacitors can be connected)

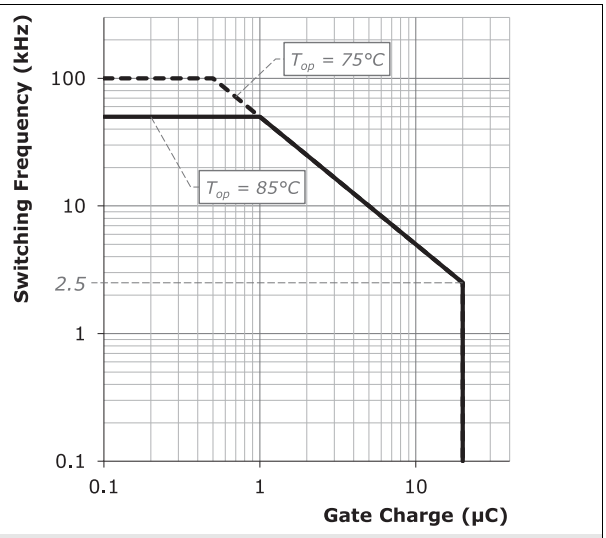


Fig. 1: Maximum Switching Frequency

IMPORTANT INFORMATION AND WARNINGS

This is an electrostatic discharge sensitive device (ESDS) according to international standard IEC 61340.

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