Technical Explanation
SKYPER® 42 LJ PV

SEMIKRON DANFOSS

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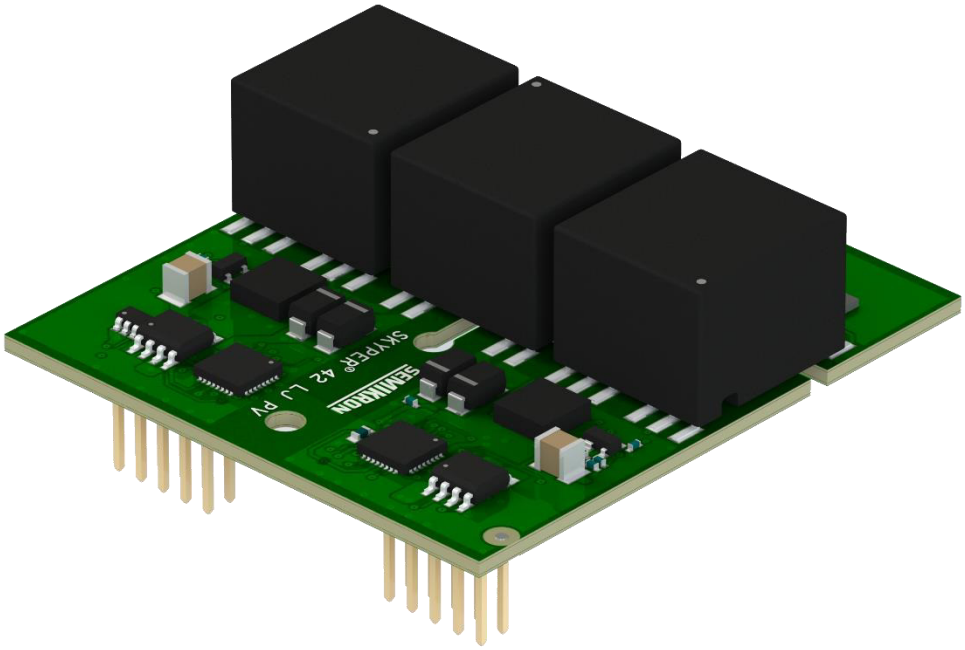
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1. Introduction

Designed to master the challenging requirements of the 7th generation IGBT semiconductor power modules, and in particular high power solar, wind, and ESS applications, the SKYPER 42 LJ PV combines SKYPER's most powerful output stages with reinforced isolation for operating voltages of up to 1500V at ambient temperatures of up to 105°C. Our highly integrated ASIC technology enables the dual-channel driver core to provide all the state-of-the-art features of the pin- and footprint-compatible industry standard driver SKYPER 42 LJ PV.
The interaction of well-tuned functionality and integrated safety functions let the driver reliably control power semiconductor modules in standard, parallel and in multi-level configurations.

Figure 1: SKYPER 42 LJ PV



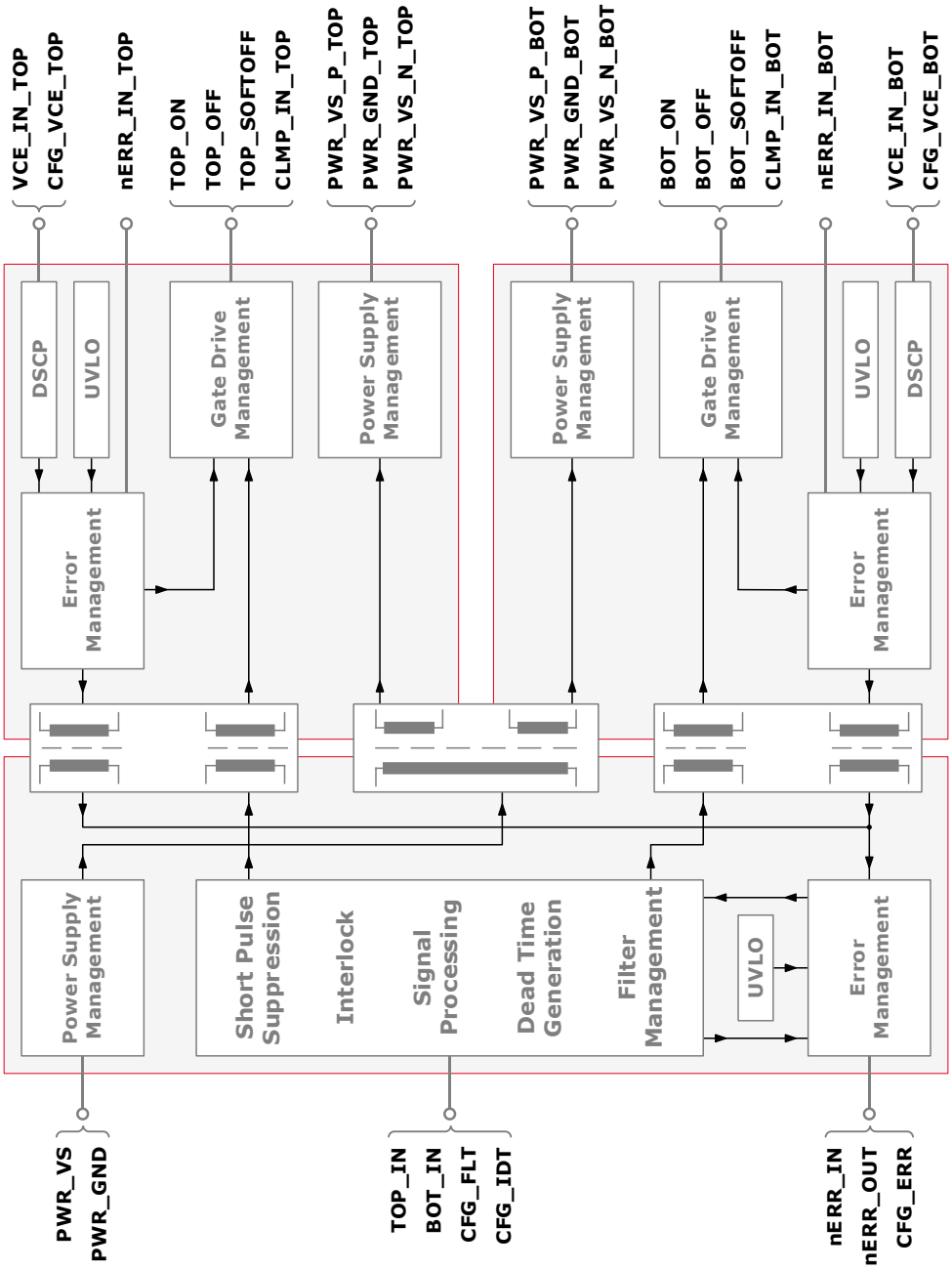
KEY FEATURES

- Two output channels
- 4.2W output power and 35A peak output current per channel
- Up to 1500V DC-Link voltage
- ±3 ns jitter per channel
- Fully isolated secondary side power supply
- Separately controlled positive and negative gate voltages
- Selectable filter settings
- Soft turn-off in case of any secondary side error event
- Short pulse suppression (SPS)
- Under voltage lockout (UVLO)
- Dynamic short circuit protection (DSCP)
- Selectable error management modes for standard and multilevel applications
- MTBF rate > 7.5 Million hours at full load

2. Block Diagram and Application Example

2.1 Block Diagram

Figure 2: SKYPER 42 LJ PV | Block diagram



2.2 Application Example

Figure 3 and **Error! Reference source not found.** show a typical SKYPER 42 LJ PV core setup to control a multilevel semiconductor module. The SKYPER 42 LJ PV employs our highly integrated ASIC chipset allowing easy configuration with only a few simple external circuits, in turn reducing the project and development time as well as the cost.

2.2.1 Primary Side

Figure 3: SKYPER 42 LJ PV | Application example | Primary side

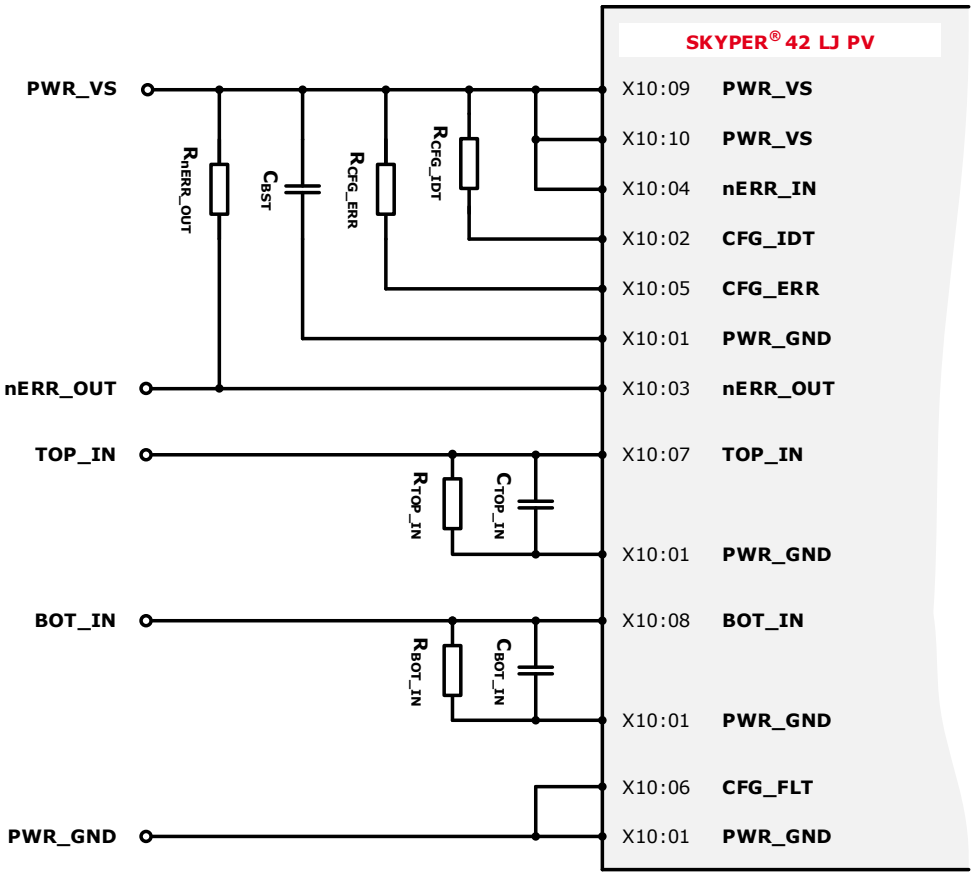


Table 1: SKYPER 42 LJ PV | Application example | Primary side | Recommended values

Component	Value	Remark
C_{TOP_IN} / C_{BOT_IN}	1nF	**Optional** filter capacitors suppressing high-frequency signals. For further information please refer to [3].
C_{BST}	-	**Optional** boost capacitor, dimensioning according to chapter 4.11.
R_{TOP_IN} / R_{BOT_IN}	10kΩ	**Optional** pull-down resistors, for steady off state of the corresponding output, if no input signal is applied.
R_{CFG_ERR} / R_{CFG_IDT}	1kΩ	**Optional.** Pull-up resistor for each configuration pins (CFG_ERR, CFG_IDT, CFG_FLT) is recommended to prevent the driver from being supplied through configuration pins. See chapter 4.12 for detailed hints.
R_{nERR_OUT}	4.75kΩ	**Optional** pull-up resistor, **necessary** if error output is used. Dimensioning according to chapter 4.6

2.2.2 Secondary Side

Figure 4: SKYPER 42 LJ PV | Application example | Secondary side

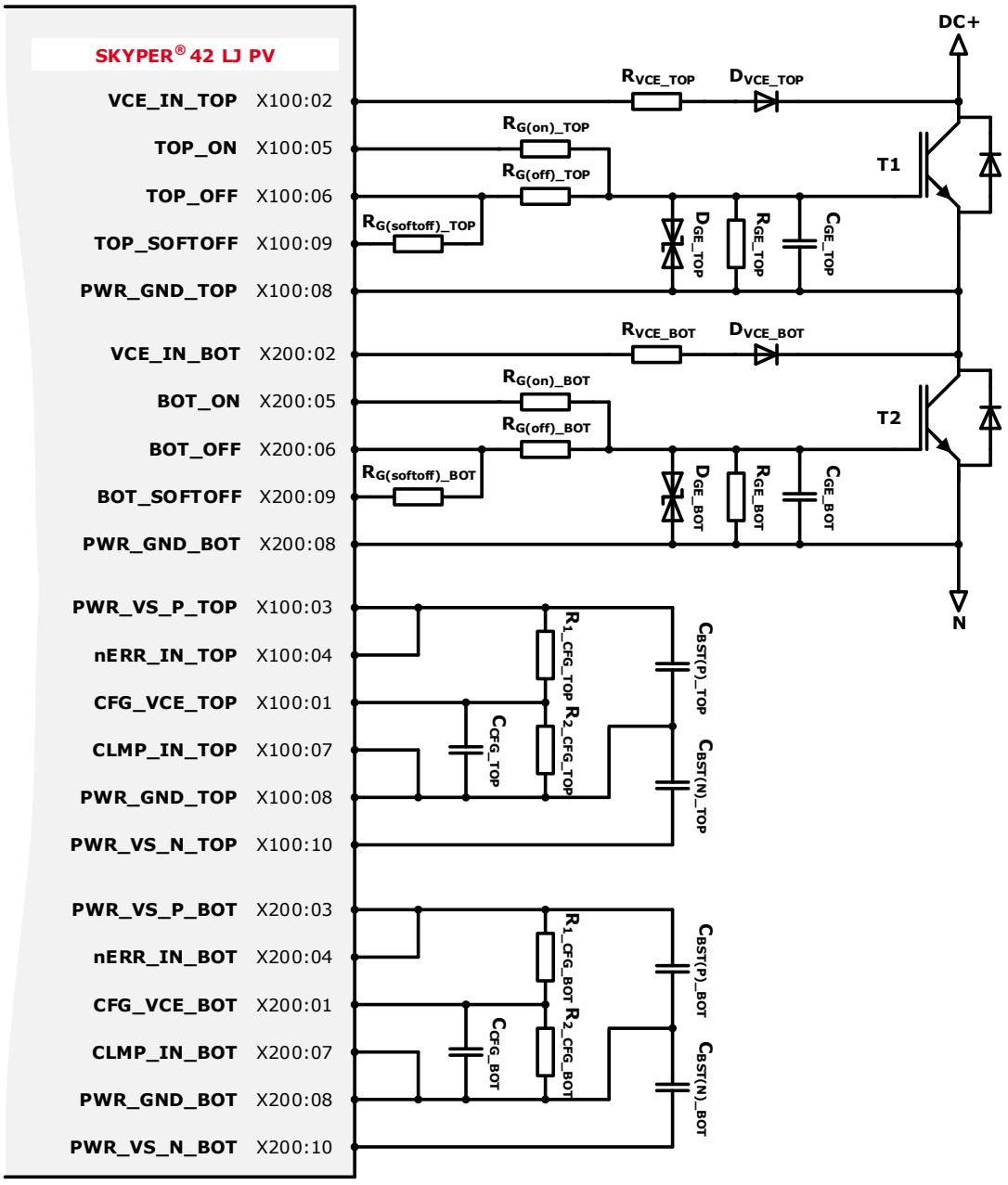


Table 2: SKYPER 42 LJ PV | Application example | Secondary side | Recommended values		
Component	**Value**	**Remark**
$C_{BST(P)_TOP}$ / $C_{BST(N)_TOP}$ $C_{BST(P)_BOT}$ / $C_{BST(N)_BOT}$	-	**Optional** boost capacitors, dimensioning according to chapter 4.11.
C_{CFG_TOP} / C_{CFG_BOT}	-	**Optional** capacitor to adjust the blanking time $t_{bl(VCE)}$ of the dynamic short circuit protection function. **Necessary** if DSCP is used. Dimensioning according to chapter 5.5.
C_{GE_TOP} / C_{GE_BOT}	-	**Optional** capacitor to prevent gate oscillation in case of short circuit events or in case of parallel operation of semiconductor power modules. For further information please refer to [3].
D_{GE_TOP} / D_{GE_BOT}	$V_{Rmin} \geq V_{G(on)} + 10\%$	**Optional** suppressor diode to prevent gate voltage overshoots. For further information please refer to [3].
D_{VCE_TOP} / D_{VCE_BOT}	-	**Optional** high voltage diode for V_{CE}-monitoring, **necessary** if DSCP is used. Dimensioning according to chapter 5.5.
$R_{1_CFG_TOP}$ / $R_{1_CFG_BOT}$	≥ 10kΩ	**Optional** resistors to adjust the trip level $V_{CE(ref)}$ of the dynamic short circuit protection, **necessary** if DCSP is used. Dimensioning according to chapter 5.5.
$R_{2_CFG_TOP}$ / $R_{2_CFG_BOT}$	-	**Optional** resistors to adjust the trip level $V_{CE(ref)}$ of the dynamic short circuit protection, **necessary** if DCSP is used. Dimensioning according to chapter 5.5.
R_{GE_TOP} / R_{GE_BOT}	10kΩ	**Optional** resistor to avoid an open gate of the semiconductor if the driver is not supplied. For further information refer to [3].
$R_{G(off)_TOP}$ / $R_{G(off)_BOT}$ $R_{G(on)_TOP}$ / $R_{G(on)_BOT}$	≥ 0.7Ω	**Necessary** resistors to adjust the semiconductors' turn-on and turn-off behavior. Dimensioning according to chapter 4.10.
$R_{G(softoff)_TOP}$ $R_{G(softoff)_BOT}$	≥ 1Ω	**Necessary** resistor to adjust the semiconductors' turn-off behavior in case of soft turn-off. Dimensioning according to chapter 4.10.
R_{VCE_TOP} / R_{VCE_BOT}	511Ω	**Optional** series resistor for V_{CE}-monitoring, **necessary** if DSCP is used.

Referring to the application example shown in Figure 3 and **Error! Reference source not found.**, Table 3 describes the settings made.

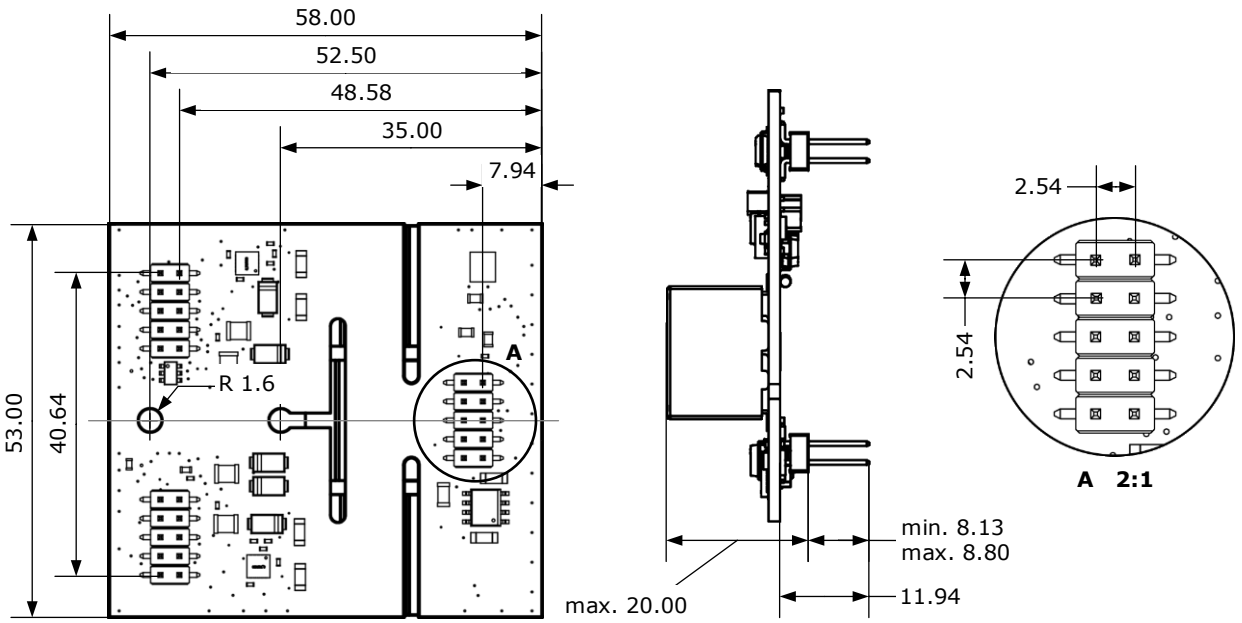
Table 3: SKYPER 42 LJ PV | Application example | Settings

Function	Configuration	Remark	Chapter
Active clamping	Disabled	Disabled by connecting the pins *CLMP_IN_TOP* and *CLMP_IN_BOT* to the corresponding *PWR_GND* pins.	5.6
Bidirectional error (=HALT)	Disabled	Disabled by connecting the pin *nERR_IN* to pin *PWR_VS*.	4.7
Dynamic short circuit protection (DSCP)	Enabled at both output channels	Enabled by connecting the pins *VCE_IN_TOP* and *VCE_IN_BOT* to the corresponding collectors of the semiconductors through R_{VCE_TOP}, D_{VCE_TOP} and R_{VCE_BOT}, D_{VCE_BOT}. DSCP configuration via pins *CFG_VCE_TOP* and *CFG_VCE_BOT*.	5.5
Dead time generation	Disabled	Disabled by connecting pin *CFG_IDT* to pin *PWR_VS*.	0
Error mode	In case of any error condition the driver reports the error event at the pin *nERR_OUT*. The driver turn-off its outputs with the next turn-off signal at the corresponding input. Both outputs remain blocked until the error state is reset.	Selected by connecting pin *CFG_ERR* to pin *PWR_VS*.	5.1
Error propagation delay time	700ns (typical value)	Fixed value.	5.1
External error	Disabled at both secondary sides.	Disabled by connecting the pins *nERR_IN_TOP* and *nERR_IN_BOT* to the corresponding *PWR_VS* pins.	5.1
Filter	Analogue	Selected by connecting pin *CFG_FLT* to pin *PWR_GND*.	5.3
Interlock	Disabled	Disabled by connecting pin *CFG_IDT* to pin *PWR_VS*.	0
Jitter	±3ns (typical value)	Selected by connecting the pin *CFG_FLT* to pin *PWR_GND*.	4.5
Short pulse suppression (SPS)	200 ns (typical value)	Selected by connecting pin *CFG_FLT* to pin *PWR_GND*.	5.3
Undervoltage lockout (UVLO)	Always active on primary and secondary side	-	5.4

3. Dimensions and mechanical precautions

3.1 Dimensions

Figure 5: SKYPER 42 LJ PV | Dimension drawing



All dimensions in mm. Please consider higher tolerances of connector position according to IPC A 610.
STEP file on request.

3.2 Plug-in connection

The SKYPER 42 LJ PV provides simple electrical and mechanical connections to adapter or control boards by its standard pin headers. The primary side and the two secondary side plug-in connectors are 10 pin dual row 2.54mm pin headers. For a secure mechanical connection of the SKYPER 42 LJ PV driver it is essential that the pin headers can be fully supported by the female mating connectors.
Example of a suitable female mating connector:

Description	Shape	Manufacturer	Art. no.
(female) RM2.54 10p	SMD 2ROW	Suyin	254100FA

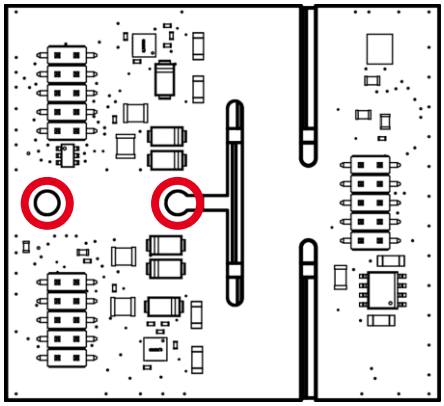
Using SMD type mating connectors allows optimized board layout, especially for spring contact modules like the SEMiX.
The SKYPER 42 LJ PV has undergone comprehensive testing comprised of profound shock and vibration tests. The SKYPER 42 LJ PV driver is approved for 3g random (10Hz … 2000Hz, 2h per axis (x, y, z)) / 5g sinusoidal (20Hz … 500Hz, 26 sweeps per axis (x, y, z), see Chapter 7. In a customer specific integration into a system the SKYPER 42 LJ PV just plugged on to a suitable receptacle on the customer's PCB would typically withstand 1g random / 3g sinusoidal. If higher robustness is required against vibration or shock, we recommend sufficiently robust mechanical support of the SKYPER 42 LJ PV PCB. This must be carefully considered in the SKYPER 42 LJ PV's integration into a user's system.

3.3 Support post

To increase the robustness of the mechanical connection between the SKYPER 42 LJ PV driver and the corresponding board, up to two support posts can be additionally assembled. It is recommended to use at least one support post. If a support post is used, make sure it has the correct length. A too short support post would bend both the driver and the corresponding board that it is mounted on, thus increasing mechanical stress. If the support post is too long, the mating connectors may not fully support the pin header and insufficient or instable electrical and mechanical contact might occur.
The mounting holes of the support posts are located in the insulation area between the secondary sides of the driver. To avoid reduction of creepage and clearance distances when utilizing a support post, the support post's material must have at least a CTI 600 classification.
Example of a support post:

Description	Shape	Manufacturer	Art. no.
Nylon support post	Dual lock	Essentra	DLMSPM-8-01 (>12mm)

Figure 6: SKYPER 42 LJ PV | Support post



mounting holes for support posts



principle of a supported driver on an adapter board

3.4 Solder connection

The SKYPER 42 LJ PV driver core can be soldered directly onto an adapter or control board. It should be noted that if the driver is placed too close to the adapter or control board, the clearance distances from the driver's primary to secondary side as well as the clearance distances between the secondary sides may be reduced.

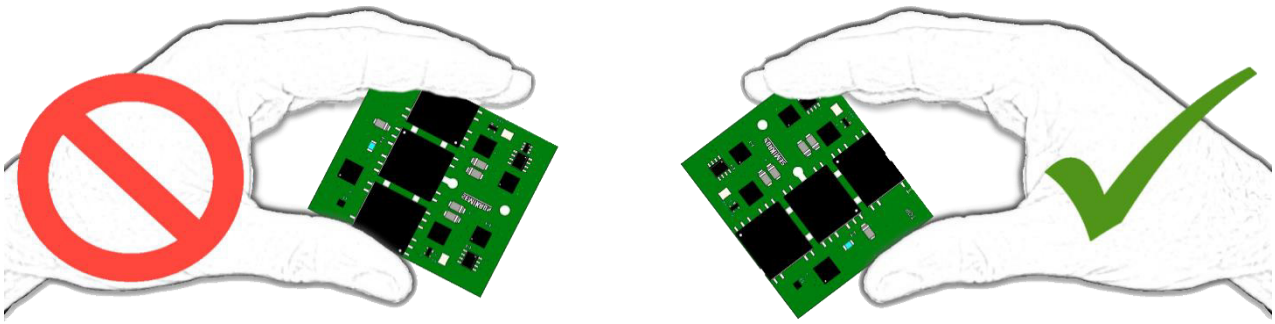
Soldering hints

- The solder's temperature must not exceed 260°C and the solder time must not exceed 10 seconds.
- The ambient temperature must not exceed the specified maximum storage temperature of the driver.
- The solder joints should be in accordance with IPC A 610 Revision D (or later) - Class 3 (Acceptability of Electronic Assemblies) to ensure an optimum connection between driver core and printed circuit board.
- The driver is not suited for hot air, reflow or infrared reflow processes.

3.5 Handling instructions

Please ensure electric static discharge protection during handling. The driver should only be removed from its original packaging just before mounting. When mounting the driver, it must be ensured that the work is done in an ESD-protected workplace environment. Persons working with the driver must wear ESD wristbands, overalls and shoes. If tools are used for mounting, those must comply with ESD standards.
When handling the driver, do not pick up the driver at the transformers. The driver MUST be handled at the PCB sides.

Figure 7: SKYPER 42 LJ PV | Handling instruction



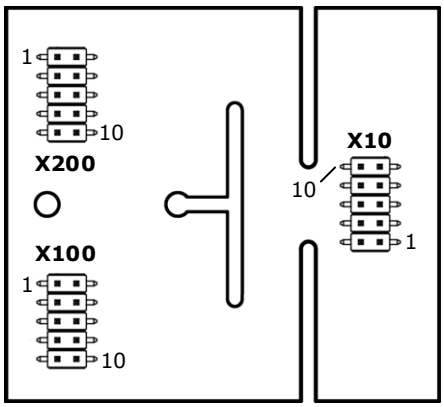
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4. Interface Description

4.1 Footprint

The footprint of the SKYPER 42 LJ PV with its primary side pin header X10 and the secondary side pin headers X100 and X200 are shown in Figure 8.

Figure 8: SKYPER 42 LJ PV | Footprint | Bottom view



4.2 Pin assignment

4.2.1 Pin assignment of pin header X10 | Primary side

Table 4: SKYPER 42 LJ PV | Pin assignment – Primary side | X10

Pin	Signal	Function	Specification
X10:01	PWR_GND	Ground potential of power supply and digital signals	To be connected to ground
X10:02	CFG_IDT	Interlock dead time configuration	15V logic; 150kΩ (pull-up) LOW = 2µs interlock dead time HIGH = No interlock dead time
X10:03	nERR_OUT	Error output	Open collector output; max. 18V/15mA (external pull-up resistor needed) LOW = Error HIGH = No error
X10:04	nERR_IN	Error input	15V logic inverted; 150kΩ/10nF (pull-up) LOW = External error HIGH = No external error
X10:05	CFG_ERR	Error behaviour configuration in case of any error condition	15V logic; 150kΩ (pull-down) LOW = Outputs switch off immediately HIGH = Outputs switch off with next turn-off signal at the corresponding input
X10:06	CFG_FLT	Filter configuration for switching signals	15V logic; 150kΩ (pull-down) LOW = Analogue filter ($t_{SPS(ana)}$) HIGH = Digital filter ($t_{SPS(dig)}$)
X10:07	TOP_IN	Switching signal input (TOP)	15V logic; 33kΩ/0.01nF (pull-down) LOW = TOP switch off HIGH = TOP switch on
X10:08	BOT_IN	Switching signal input (BOT)	15V logic; 33kΩ/0.01nF (pull-down) LOW = BOT switch off HIGH = BOT switch on
X10:09	PWR_VS	Driver power supply	Stabilised +15V ±4%

X10:10	PWR_VS	Driver power supply	Stabilised +15V ±4%

4.2.2 Pin assignment of pin header X100 | Secondary side | TOP

Table 5: SKYPER 42 LJ PV | Pin assignment – Secondary side | TOP | X100

Pin	Signal	Function	Specification
X100:01	CFG_VCE_TOP	V_{CE}-monitoring reference voltage	External voltage divider needed
X100:02	VCE_IN_TOP	V_{CE}-monitoring input	External blocking diode needed
X100:03	PWR_VS_P_TOP	Power supply output, positive voltage	Equal to $V_{G(on)}$ [1)] (external buffer capacitors can be optionally connected)
X100:04	nERR_IN_TOP	External error input	15V logic inverted; 150kΩ/0.01nF (pull-up) LOW = External error HIGH = No external error
X100:05	TOP_ON	On signal terminal for TOP semiconductor	External gate resistor needed (under consideration of $I_{out(avg)}$, $I_{out(peak)}$, $V_{G(on)}$)
X100:06	TOP_OFF	Off signal terminal for TOP semiconductor	External gate resistor needed (under consideration of $-I_{out(avg)}$, $-I_{out(peak)}$, $V_{G(off)}$)
X100:07	CLMP_IN_TOP	V_{CE}-clamping input	150kΩ/0.01nF (pull-down) In case of activated TOP_OFF: LOW = TOP_OFF equal to $V_{G(off)}$ HIGH = TOP_OFF floating
X100:08	PWR_GND_TOP	Ground potential of power supply and digital signals	Reference potential of gate voltages (emitter/source of power semiconductor)
X100:09	TOP_SOFTOFF	SoftOff signal terminal for TOP semiconductor	External gate resistor needed
X100:10	PWR_VS_N_TOP	Power supply output, negative voltage	Equal to $V_{G(off)}$ [1)] (external buffer capacitors can be optionally connected)

[1)] Unsymmetrical load between PWR_VS_P_TOP to PWR_GND_TOP and PWR_VS_N_TOP to PWR_GND_TOP should be avoided.

4.2.3 Pin assignment of pin header X200 | Secondary side | BOT

Table 6: SKYPER 42 LJ PV | Pin assignment – Secondary side | BOT | X200

Pin	Signal	Function	Specification
X200:01	CFG_VCE_BOT	V_{CE}-monitoring reference voltage	External voltage divider needed
X200:02	VCE_IN_BOT	V_{CE}-monitoring input	External blocking diode needed
X200:03	PWR_VS_P_BOT	Power supply output, positive voltage	Equal to $V_{G(on)}$ [1)] (external buffer capacitors can be optionally connected)
X200:04	nERR_IN_BOT	External error input	15V logic inverted; 150kΩ/0.01nF (pull-up) LOW = External error HIGH = No external error
X200:05	BOT_ON	On signal terminal for BOT semiconductor	External gate resistor needed (limits under consideration of $I_{out(avg)}$, $I_{out(peak)}$, $V_{G(on)}$)
X200:06	BOT_OFF	Off signal terminal for BOT semiconductor	External gate resistor needed (limits under consideration of $-I_{out(avg)}$, $-I_{out(peak)}$, $V_{G(off)}$)

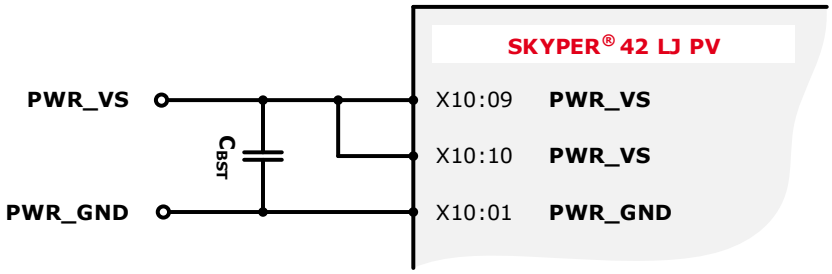
X200:07	CLMP_IN_BOT	V_{CE}-clamping input	150kΩ/0.01nF (pull-down) In case of activated BOT_OFF: LOW = BOT_OFF equal to $V_{G(off)}$ HIGH = BOT_OFF floating
X200:08	PWR_GND_BOT	Ground potential of power supply and digital signals	Reference potential of gate voltages (emitter/source of power semiconductor)
X200:09	BOT_SOFTOFF	SoftOff signal terminal for BOT semiconductor	External gate resistor needed
X200:10	PWR_VS_N_BOT	Power supply output, negative voltage	Equal to $V_{G(off)}$ [1)] (external buffer capacitors can be optionally connected)

[1)] Unsymmetrical load between PWR_VS_P_BOT to PWR_GND_BOT and PWR_VS_N_BOT to PWR_GND_BOT should be avoided.

4.3 Power supply | Primary side

For a proper operation of the SKYPER 42 LJ PV driver core, a power supply of at least 15W/1.5A shall be connected to the driver's power supply pins. During power-up of the driver turn-on signals should not be applied to the driver's inputs *TOP_IN/BOT_IN*, otherwise the driver will not leave the error state.
Please note, when controlling power semiconductor modules with a gate charge ≥ 2.5 µC external boost capacitors (C_{BST}) are recommended to support the supply voltage on the primary side. Dimensioning of the boost capacitors shall be done according to chapter 4.11.

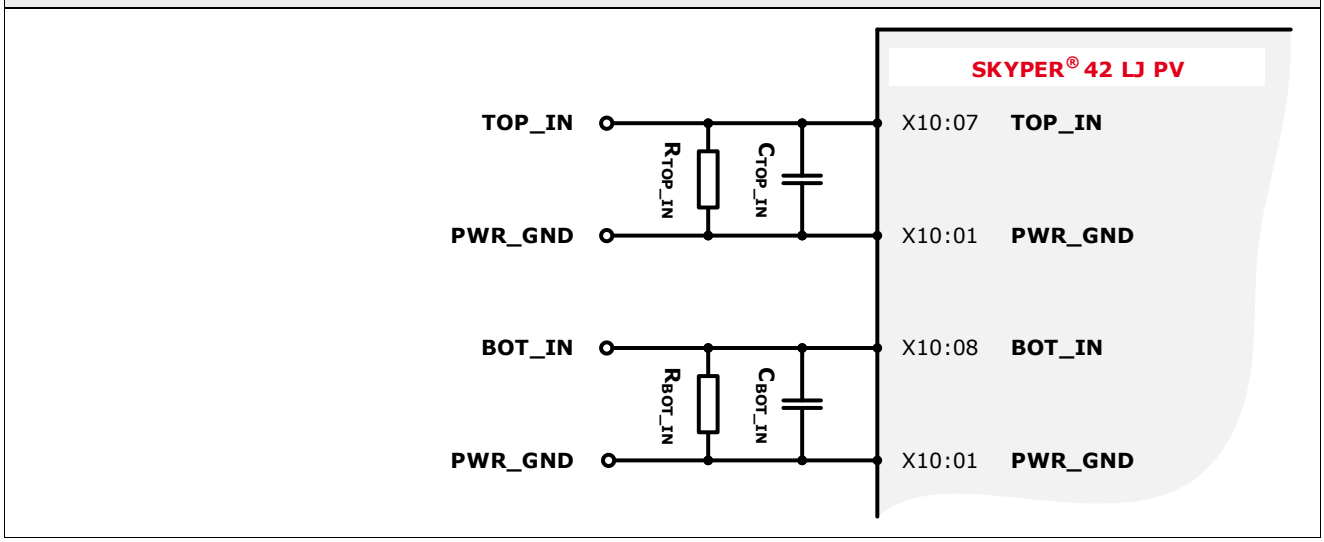
Figure 9: SKYPER 42 LJ PV | Primary side | Power supply



4.4 Gate drive signals | Primary side

The signal inputs *TOP_IN/BOT_IN* of the SKYPER 42 LJ PV driver core have +15V Schmitt trigger logic. A HIGH signal at the input of the driver turns on the corresponding output of the driver. A LOW signal at the input leads to a switch-off command at the corresponding output. Pulses below 1µs are not allowed.
Short pulses as well as voltage peaks, e.g. caused by interference, are suppressed by the driver, and will not be transmitted to the outputs. Further information on the short pulse suppression is found in chapter 5.3.

Figure 10: SKYPER 42 LJ PV | Primary side | Gate drive signals



When using the driver in environments with high levels of electromagnetic noise, it is recommended to connect a filter capacitor (C_{TOP_IN}/C_{BOT_IN}) of several hundred picofarads as closely as possible to the signal inputs. Please note that these capacitors affect the propagation delay time of the driver. The R_{TOP_IN}/R_{BOT_IN} resistors pull the inputs to low-level when no control signals are applied. The recommended value of the pull-down resistors is approximately 10kΩ.

Parameter	Min	Typ	Max
Threshold high	-	-	10V
Threshold low	5V	-	-

4.5 Filter selection, Jitter and propagation delay time | Primary side

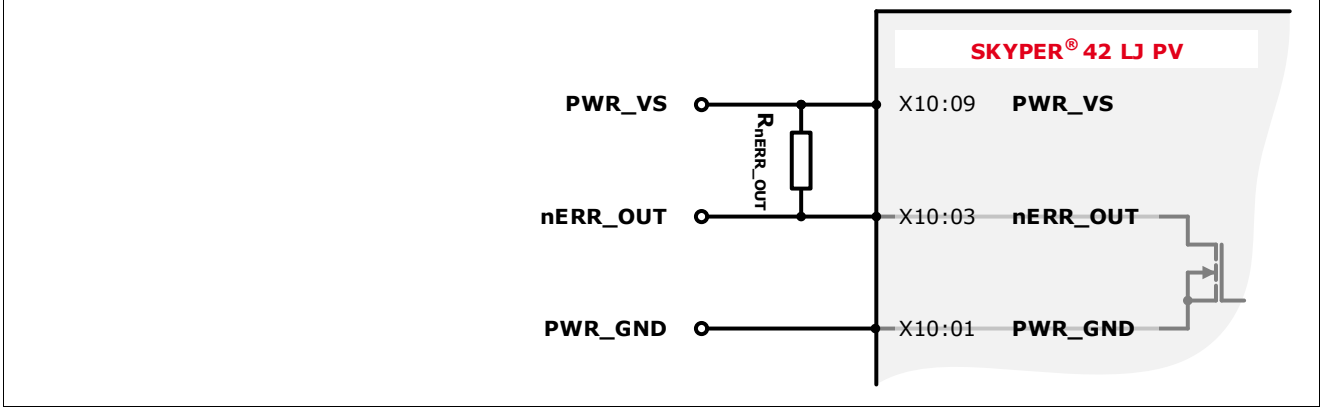
Our highly integrated mixed signal ASICs the SKYPER 42 LJ PV permit the selection of filter type, jitter, and propagation delay time to meet specific requirements of the application.
The filter time can be set via the configuration pin *CFG_FLT*. Connecting the *CFG_FLT* pin to the *PWR_VS* pin enables the digital filter employing very low tolerances over the full temperature range.
Depending on the settings made, the SKYPER 42 LJ PV driver provides a very low jitter of typically ±3ns. When using this mode, the analogue filter must be enabled, and the driver's internal dead time generator must be set inactive. The dead time generator is inactive if either the interlock feature is disabled via the *CFG_IDT* pin or the dead time of the applied pulse pattern is longer than 2µs. A detailed description of the interlock function and the dead time generation is found in chapter 0.

CFG_FLT	*CFG_IDT*	Setting	Filter time	Delay time	Jitter
HIGH	HIGH/LOW	Digital filter	390ns	830ns	±12.5ns
LOW	LOW	Analogue filter	200ns	500ns	±3ns /±12.5ns
LOW	HIGH	Analogue filter	200ns	500ns	±3ns

4.6 Error output | Primary side

The SKYPER 42 LJ PV reports any detected error event at the *nERR_OUT* pin by pulling it to low-level. The error output is an open collector output and requires an external pull-up resistor (R_{nERR_OUT}). The recommended value of the pull-up resistor is in the range of $PWR_VS/I_{max,nERR_OUT} \leq R_{nERR_OUT} \leq 10k\Omega$.
As long as the driver has not been reset the error output will be at low-level.
A detailed description, how to reset the driver to exit the error state and resume to operation is described in chapter 5.1.

Figure 11: SKYPER 42 LJ PV | Primary side | Error output

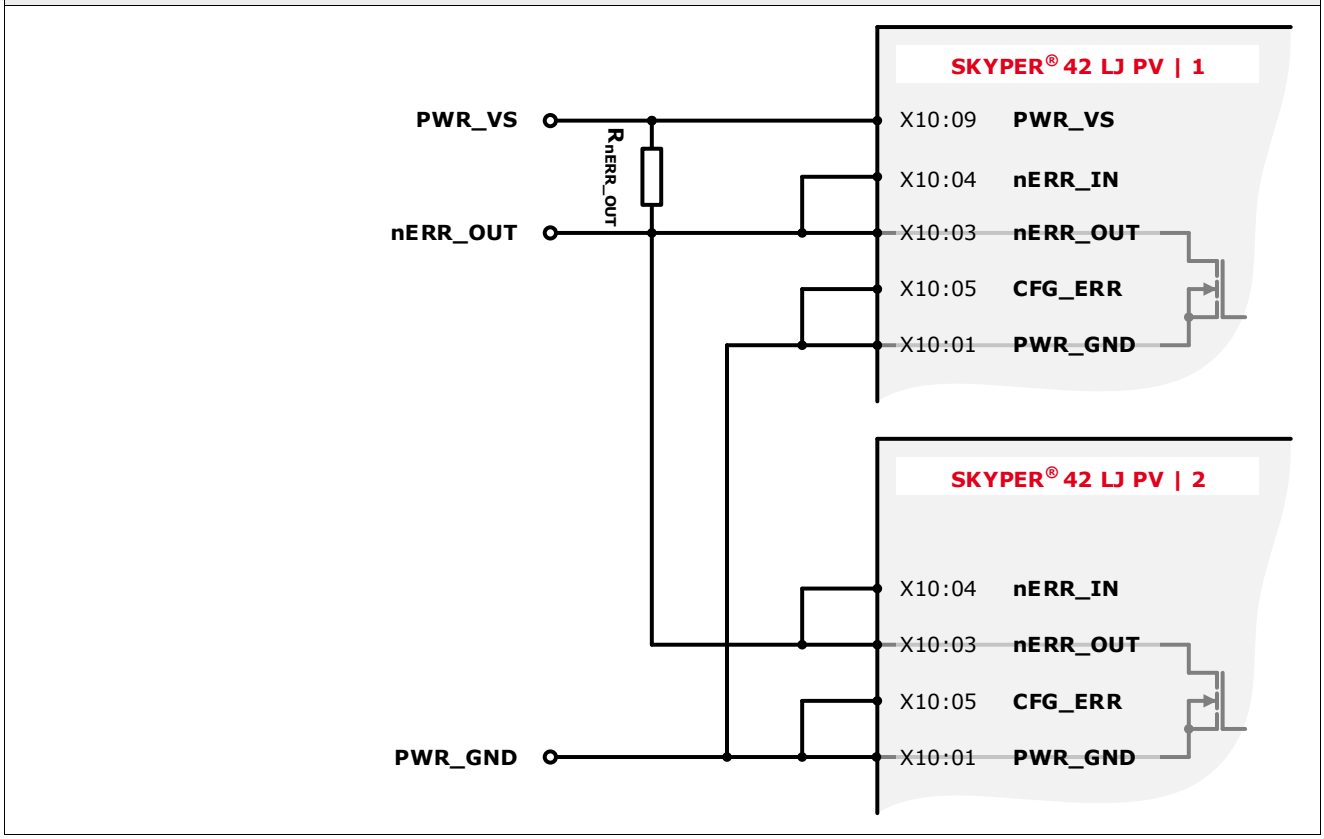


Please note, if the *nERR_OUT* terminal of SKYPER 42 LJ PV is directly connected to a *nERR_OUT* terminal of another SKYPER 42 LJ PV driver, only one pull-up resistor must be applied.

4.7 Error input | Primary side

The *nERR_IN* is optionally used to report a system related external error event to the SKYPER 42 LJ PV. If the *nERR_IN* input is pulled down to low-level the driver enters an error state. Depending on the error mode configuration, described in chapter 4.8, the driver sets its outputs either immediately or with the next turn-off command at its corresponding input to low-level and locks them. After reset, as described in chapter 5.1, the driver will be ready to transfer the signals to the output stage, again. If no reporting to the external error input is required, the *nERR_IN* input can be connected to the *PWR_VS* pin or to the *nERR_OUT* pin.
In multiphase or parallel operation, the *nERR_IN* input offers the possibility to force the outputs of each driver in the system to off-state and locks them, simultaneously, without the need of an external control unit. Therefore, all *nERR_OUT* outputs and all *nERR_IN* inputs must be connected together forming a common bi-directional HALT line. Additionally, all *CFG_ERR* configuration pins must be connected to ground potential, as shown in Figure 12. In this configuration, any driver connected to the HALT line can force the outputs of all connected drivers to off-state and locks them, when the driver pulls its *nERR_OUT* output to low-level.
If a specific turn-off sequence is required – as it is common practice in NPC multilevel applications – the configuration pins *CFG_ERR* must be connected to the *PWR_VS* pins. A low-level of the HALT line locks the outputs of the connected drivers but does not immediately force them to low-level. Outputs which are in on-state can be forced to off-state by the controller sending a turn-off command to the corresponding signal inputs *TOP_IN/BOT_IN*.
If the driver is used in environments with high levels of EMI noise, it is recommended to connect an additional filter capacitor as closely as possible to the *nERR_IN* pin and the *PWR_GND* pin.

Figure 12: SKYPER 42 LJ PV | Primary side | Error input



Parameter	Min	Typ	Max
Threshold high	-	-	11 V
Threshold low	7.5 V	-	-

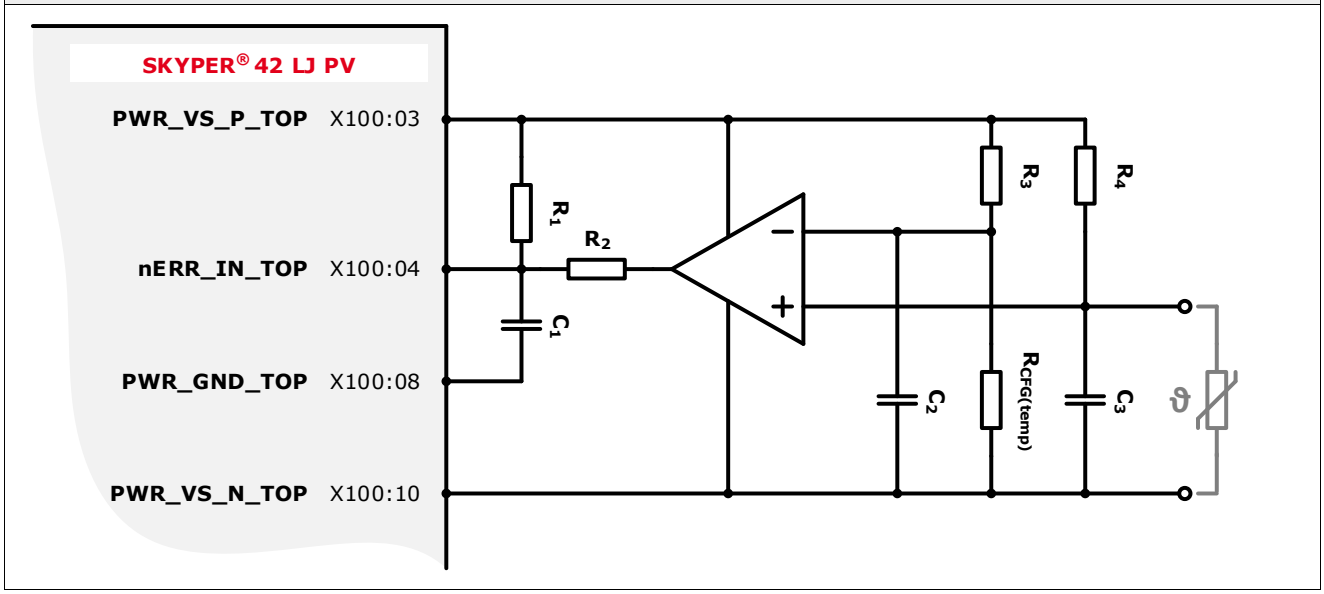
4.8 Error mode selection | Primary side

The configuration pin *CFG_ERR* selects behaviour of the SKYPER 42 LJ PV driver core in case of error events. Connecting the *CFG_ERR* pin to the *PWR_GND* pin forces the driver to set its outputs to off-state immediately when an error is detected. As long as the driver has not been reset the error event is reported at the corresponding output and the driver's outputs are locked. Whereby, depending on whether an error is detected on the primary or on the secondary side the driver switches off the connected semiconductors via the standard turn-off or the soft-off path. If an error occurs on the primary side the driver will activate the standard turn-off paths of both channels. If an error occurs on the secondary side, the driver will activate the soft-off path of the affected secondary side. The semiconductor connected to the other secondary side will be switched off via the standard turn-off path.
If the *CFG_ERR* pin is connected to the *PWR_VS* pin, the driver locks its outputs in case of any error event's occurrence and, hence, reports the error event at the terminal *nERR_OUT*. The outputs will be set to off-state when the driver has received a turn-off command at the corresponding signal input *TOP_OFF/BOT_OFF*. Depending on whether an error is detected on the primary or secondary side the driver activates the standard turn-off or the soft-off path, as described above.
Further information related to the primary and secondary side error events, as well as on the error reset conditions is found in chapter 5.1.
Please see chapter 4.12 for details on configuration pins connections.

4.9 External error input | Secondary side

Each secondary side of the driver provides an error input (*nERR_IN_TOP/nERR_IN_BOT*) to handle external error events. These inputs are low active. Pulling one input to low-level forces the driver into an error state. The behaviour of the driver in case of an external error event depends on the configuration at the configuration pin *CFG_ERR*, as described in chapter 4.8.
The external error input is typically used to monitor temperature, current or voltage of modules, phase legs or systems. The error input of the secondary TOP/BOT side can be disabled by connecting it to the *PWR_VS_P_TOP/PWR_VS_P_BOT* pin.
Figure 13 shows a recommended comparator circuitry to process the NTC's signal and derive the required logic signal for the input of the SKYPER 42 LJ PV. When the voltage at the comparator's positive input falls below the voltage level of the negative input the *nERR_IN* input will be pulled to low-level and generates an external error event. Assuming that resistors R_3 and R_4 have the same value the comparator's trip level is reached when the value of the NTC falls below the value of $R_{CGF(temp)}$. Please note that the negative supply pin of the comparator is connected to *PWR_VS_N* which must be taken into account, in case the NTC thermistor is also monitored by an external application circuit in addition.

Figure 13: SKYPER 42 LJ PV | Secondary side | Example of an external error input circuitry



Recommended values		
Component	**Value**	**Remark**
C_1	1nF	
C_2	100nF	
C_3	1µF	
R_1	30.1kΩ	
R_2	15kΩ	
R_3	30.1kΩ	
R_4	30.1kΩ	
$R_{CFG(temp)}$	-	The value of the resistor $R_{CFG(temp)}$ must be determined considering the resistance characteristic of the connected thermistor and the desired trip level.

Parameter	Min	Typ	Max
Threshold high	-	-	13 V
Threshold low	2 V	-	-

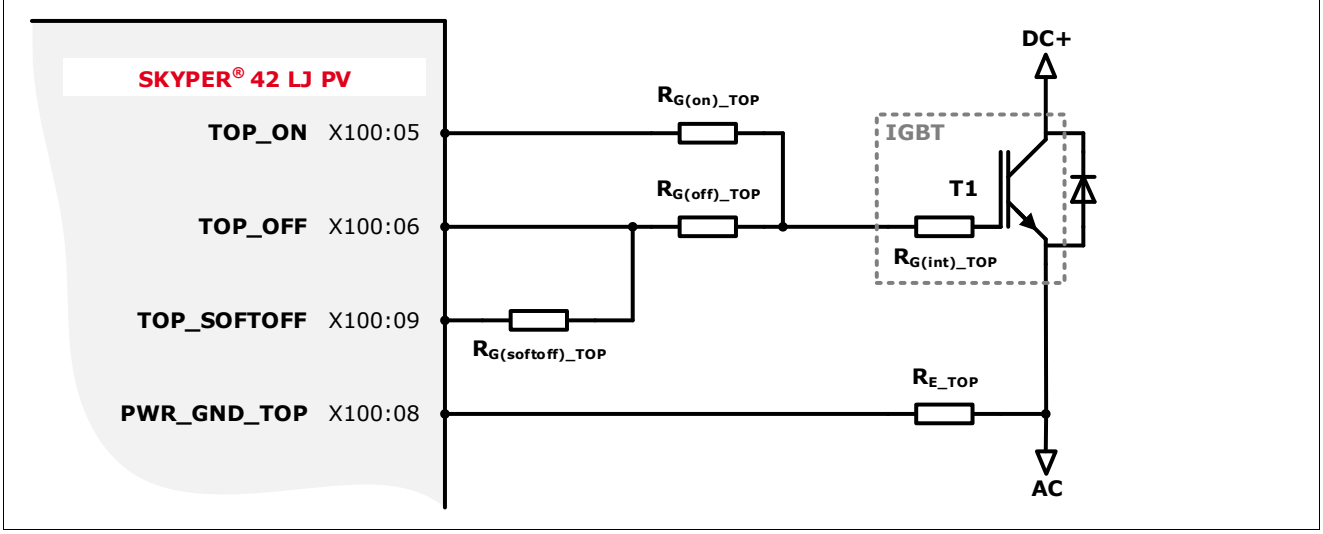
4.10 Gate resistors | Secondary side

Equipped with three output channels on each secondary side (*TOP_ON/TOP_OFF/TOP_SOFTOFF* and *BOT_ON/BOT_OFF/BOT_SOFTOFF*) the SKYPER 42 LJ PV driver offers the possibility to optimize turn-on and turn-off behavior of the IGBT separately. By default, the driver uses the *TOP_ON/TOP_OFF* and *BOT_ON/BOT_OFF* output to turn-on or turn-off the connected semiconductor. The SOFTOFF output will be activated by the driver if a secondary side error event has been detected to turn-off of the connected semiconductor slowly, which in turn shall prevent from excessive voltage overshoots to protect the semiconductor against destruction by over voltage. It is mandatory to populate a suitable soft-off gate resistor, otherwise the semiconductor will not be turned-off in case of a secondary side error. A detailed explanation of when the driver is activating the soft-off path is referred in chapter 4.8.
The gate resistor influences the IGBT switching time, switching losses, reverse bias safe operating area (RBSOA), short-circuit safe operating area (SCSOA), EMI, dV/dt, di/dt and reverse recovery current of the freewheeling diode. The gate resistor essentially optimizes the safe operation of the power semiconductor to the individual application parameters, e.g. IGBT technology, diode, switching frequency, losses, application layout, inductivity / stray inductance, DC-link voltage, and driver capability. The complete design of an application must be viewed as a whole, with due considering of the above-mentioned parameters at least. Interacting and interfering effects within the whole application must be considered, evaluated, and addressed. [4]
The minimum allowed value of the gate resistors $R_{G(on)}$ and $R_{G(off)}$ can be calculated by the following equation:

$$R_{G(\min)} = R_G + R_{G(int)} + R_E = \frac{V_{G(on)} - V_{G(off)}}{I_{out(peak)}}$$

The minimum permissible value of the $R_{G(softoff)}$ is 1Ω. Additional hints how to determine the values of the gate resistors are found in [4].

Figure 14: SKYPER 42 LJ PV | Secondary side | Gate resistors



Please note that some of our driver cores using an N-channel MOSFET for Soft Off that is contained within the ASIC. To protect this MOSFET against stress when turning-off the TOP_ON/BOT_ON channel it is recommended to place the $R_{G(softoff)}$ resistor in series with the $R_{G(off)}$ resistor.
Since each turn-on and turn-off of a semiconductor means charging or discharging the input capacitance of the connected power semiconductor, the gate resistor must be suitable for pulsed loads. For this reason, it is recommended to use pulse current rated resistors. The following table provides examples:

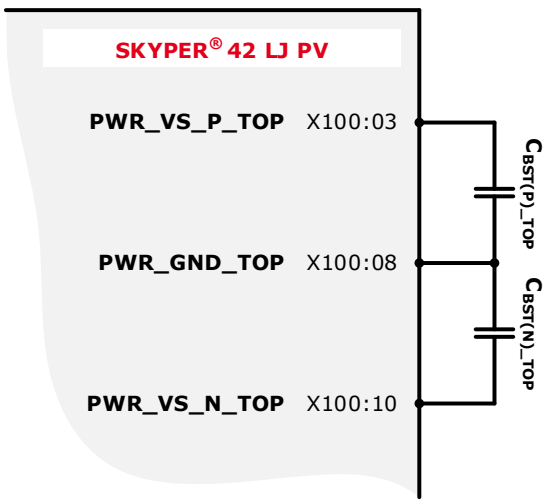
Description	Shape	Manufacturer	Art. no.
MELF resistors	MELF / MiniMELF SMD	Vishay Beyschlag, Vishay Draloric, Vitrohm	PRO MELF resistors, SMM0207, SMM 0204, ZCM series

4.11 External boost capacitors | Secondary side

The SKYPER 42 LJ PV allows driving of semiconductor power modules with a gate charge (Q_G) of up to 20µC per channel. If the gate charge of the connected module is larger than 2.5µC, the use of boost capacitors for each output channel is recommended to stabilize the gate voltages $V_{G(on)}$ and $V_{G(off)}$ during switching. For

maximum effectiveness, these capacitors must be placed as closely as possible to the corresponding terminal, as shown in Figure 15.

Figure 15: SKYPER 42 LJ PV | Secondary side | Boost capacitors



The required capacitance of the optional external boost capacitors can be estimated by following the equation:

$$C_{BST(P)} = C_{BST(N)} = A \times Q_G - 10\mu F \qquad for\ 2.5\mu C < Q_G \leq 20\mu C$$

$$A = 5 \ldots 7 \frac{\mu F}{\mu C} \qquad IGBT\ 7\ module$$

$$A = 4 \frac{\mu F}{\mu C} \qquad IGBT\ module$$

Please note, when assembling boost capacitors on the secondary sides, boost capacitors must also be assembled on the primary side (C_{BST}), as shown in Figure 9.

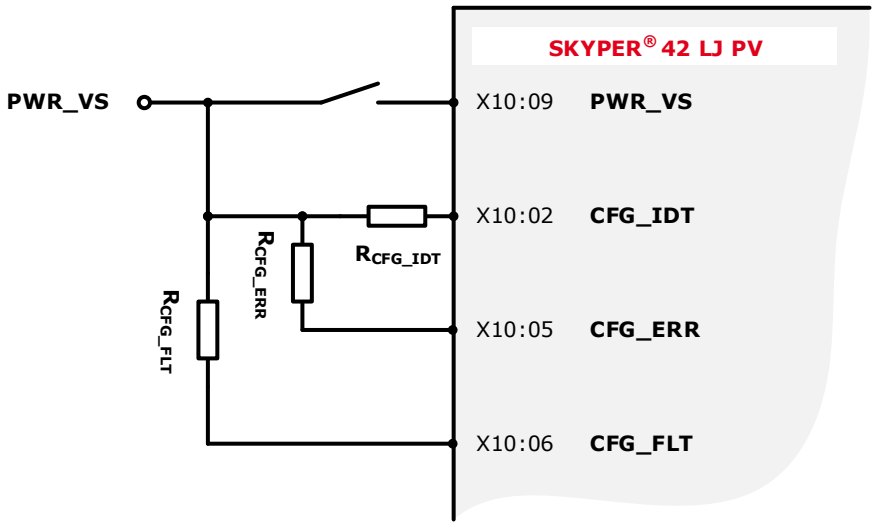
$$C_{BST} = C_{BST(P)} = C_{BST(N)}$$

4.12 Configuration pins | Primary side

The configuration pins for the dead time *CFG_IDT*, error behaviour *CFG_ERR,* and filter option *CFG_FLT* may be set to HIGH or LOW depending on which configurations are intended, as described in chapters 4.5 and 4.8. To ensure that the driver will not be supplied through the configuration pins, a decoupling resistor of 1kΩ is recommended to be placed between supply and each configuration pin. Please refer to the example in Figure 16 below.

Exception: If the configuration pins are directly connected to PWR_VS (x10:09 and/or X10:10), the mentioned resistors can be omitted.

Figure 16: SKYPER 42 LJ PV | Primary side | Configuration Pins



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5. Protection features

5.1 Failure management

The SKYPER 42 LJ PV driver core detects several different error events on primary and secondary sides. The driver's reaction on those events depends on the selected error mode, as described in chapter 4.8. The following table covers the possible error routine scenarios.

Table 7: SKYPER 42 LJ PV | Failure management

Conditions			Reaction		
Error event	**Occurrence**	***CFG_ERR***	***nERR_OUT***	**Outputs**	**Turn-off path**
Undervoltage of power supply	primary side	HIGH/LOW	LOW immediately	OFF and locked, immediately, until reset	Standard
nERR_IN at low-level	primary side	HIGH	LOW immediately	OFF, with next turn-off signal at the corresponding input Locked immediately OFF & locked until reset	Standard
		LOW	LOW immediately	OFF and locked, immediately, until reset	Standard
Undervoltage of power supply	secondary side	HIGH	LOW immediately	OFF, with next turn-off signal at the corresponding input Locked immediately OFF & locked until reset	Soft Off affected channel Standard not affected channel
		LOW	LOW immediately	OFF and locked, immediately, until reset	
Short circuit detection (DSCP)	secondary side	HIGH	LOW immediately	OFF, with next turn-off signal at the corresponding input Locked immediately OFF & locked until reset	Soft Off affected channel Standard not affected channel
		LOW	LOW immediately	OFF and locked, immediately, until reset	
nERR_IN at low-level	secondary side	HIGH	LOW immediately	OFF, with next turn-off signal at the corresponding input Locked immediately OFF & locked until reset	Soft Off affected channel Standard not affected channel
		LOW	LOW immediately	OFF and locked, immediately, until reset	

If the SKYPER 42 LJ PV has entered the error state, it must be reset before the driver resumes to operation mode. The driver could be reset under the following conditions:

- >30µs non-error condition (Reaction on customer side should happen within that time)
- >9µs no input signals at *TOP_IN/BOT_*IN (Customer confirms error)

After completing the reset sequence, the driver returns 'ready for operation' by setting the *nERR_OUT* output to high-level.

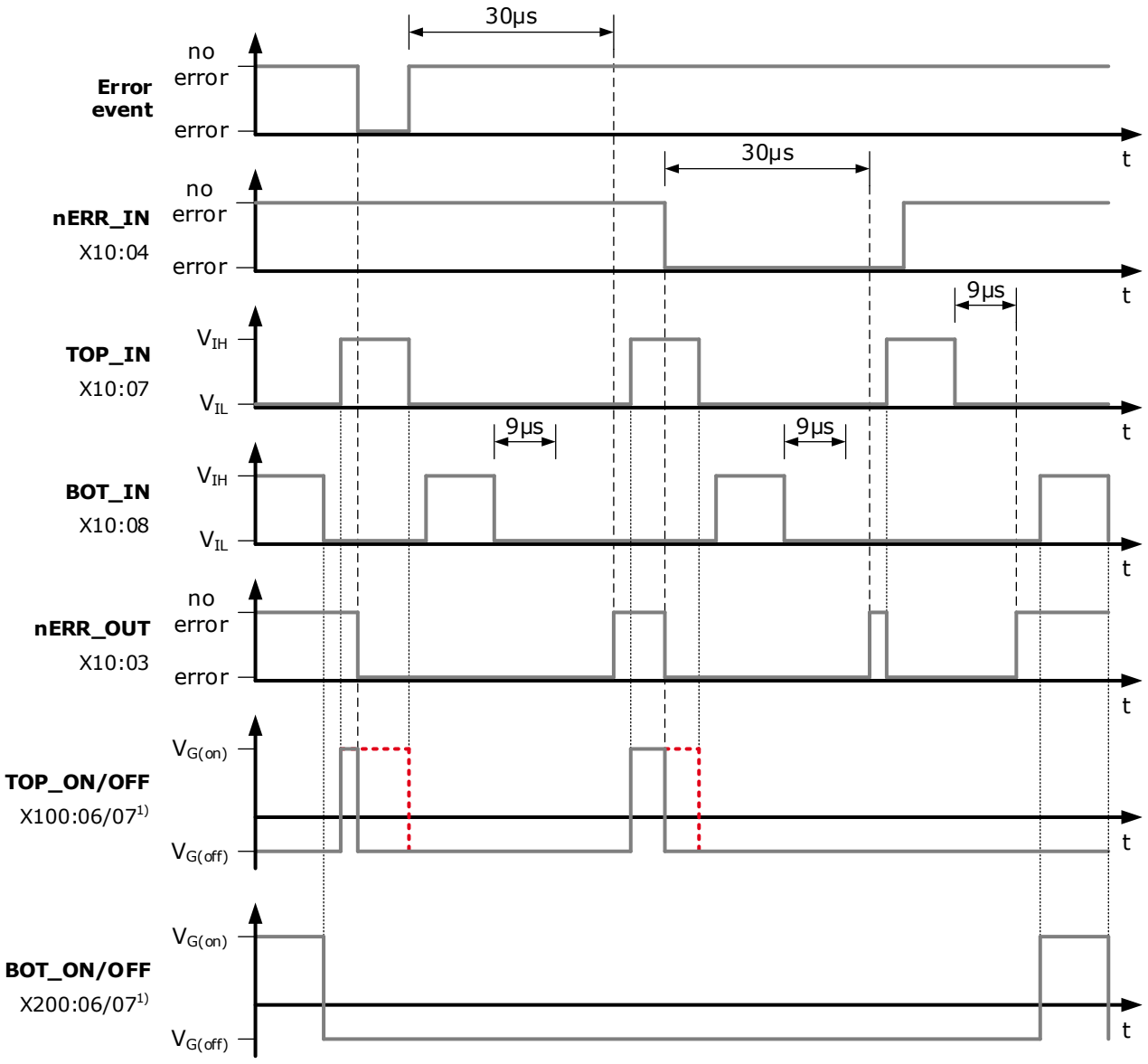
If the driver has entered error state because of an externally reported error event by the controller via the primary side *nERR_IN* pin, the driver can be reset under the following conditions:

- 30µs has elapsed until the external error event occurred
- > 9µs no input signals at *TOP_IN/BOT_IN*

Important note
If the *nERR_OUT* output is set to high-level by the driver and the external error signal is removed, the driver is ready for operation again. This behaviour prevents deadlock situations if several drivers are using the bi-directional HALT feature, as described in chapter 4.7.

The behavior of the driver on an error event is also shown in Figure 17. The red dotted lines show the behavior of the driver, if the error configuration pin *CFG_ERR* is connected to *PWR_VS*.

Figure 17: SKYPER 42 LJ PV | Behavior on error event



1) The signal characteristics of BOT_ON/OFF and TOP_ON/OFF are valid if the outputs X100:06 and X100:07, also X200:06 and X200:07, are connected to each other through gate resistors.

5.2 Dead Time and Interlock

The internal dead time generation of the SKYPER 42 LJ PV as well as the interlock feature can be selected via the configuration pin *CFG_IDT*. The following modes are available:

- Interlock enabled, 2µs dead time
- Interlock disabled, no dead time

Interlock enabled

To enable the interlock feature the *CFG_IDT* pin must be connected to *PWR_GND*. The interlock feature is typically used when driving power semiconductor modules in half bridge configuration. The feature prevents the two outputs from being activated simultaneously, which would lead to a shorted DC-link connection (bridge shoot through). The interlock feature also allows controlling a power semiconductor module with one switching signal and its inverted signal at the driver's inputs *TOP_IN/BOT_IN*.

The internal timer which generates the dead time, starts with each turn-off command at the inputs *TOP_IN/BOT_IN*. If the dead time of 2µs has not elapsed, the driver locks the other output. If the pulse pattern generated by the customer's controller also includes a dead time, the resulting system dead time will be determined by either the controller or the driver, depending on whichever dead time duration is longer. The SKYPER 42 LJ PV does not add the internal generated dead time to the dead time of the pulse pattern of the controller.

Interlock disabled

If the interlock feature is disabled by connecting the configuration pin *CFG_IDT* to the *PWR_VS* pin, both outputs of the driver can be switched independently from each other. Hence, both output channels could be switched-on at the same time without blocking.
Table 8 shows the resulting system dead time depending on the configuration via the *CFG_IDT* pin.

Table 8: SKYPER 42 LJ PV | Resulting system dead time

CFG_IDT	Interlock	Controller dead time	SKYPER dead time	Resulting dead time
LOW	Enabled	No dead time	2µs	2µs
LOW	Enabled	< 2µs	2µs	2µs
LOW	Enabled	> 2µs	2µs	> 2µs
HIGH	Disabled	2µs	No dead time	2µs
HIGH	Disabled	No dead time	No dead time	No dead time

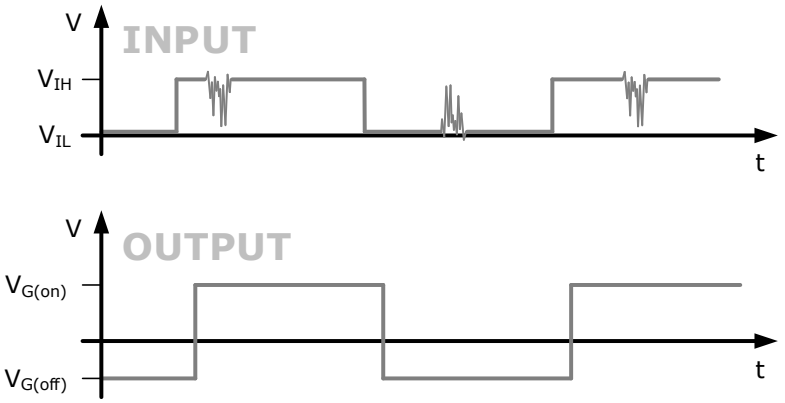
Important Note

When the interlock function is disabled a bridge shoot through must be prevented by the user's control unit.

5.3 Short pulse suppression (SPS)

The SKYPER 42 LJ PV driver suppresses short on- and off-pulses on the signal inputs *TOP_IN/BOT_IN* and, hence, enhances the interference ruggedness. The time of suppression corresponds to the filter time set by the customer via the configuration pin *CFG_FLT*, as described in chapter 4.5.

Figure 18: SKYPER 42 LJ PV | Short Pules Suppression



5.4 Undervoltage lockout (UVLO)

The SKYPER 42 LJ PV driver permanently monitors the supply voltage of the primary side as well as both positive and both negative gate voltages of the secondary sides. If either the supply voltage or a positive gate voltage drops below the 'shutdown' threshold levels the driver enters an error state. The same applies when a negative gate voltage exceeds the 'shutdown' threshold level. Once entered into an error state the driver executes its error routine as described in chapter 5.1.
The error condition resets when the supply voltage and both positive gate voltages have exceeded the 'non-error' threshold level and both negative gate voltages have dropped below the 'non-error' threshold level. The driver will be ready again for operation after reset, as described in chapter 5.1

Parameter	Min	Typ	Max
Primary side shutdown threshold	12.6V		
Primary side non-error threshold			13.8V
Secondary side shutdown threshold, positive gate voltage	9.4V		
Secondary side non-error threshold, positive gate voltage			13.3V
Secondary side shutdown threshold, negative gate voltage			-4.1V
Secondary side non-error threshold, negative gate voltage	-5.8V		

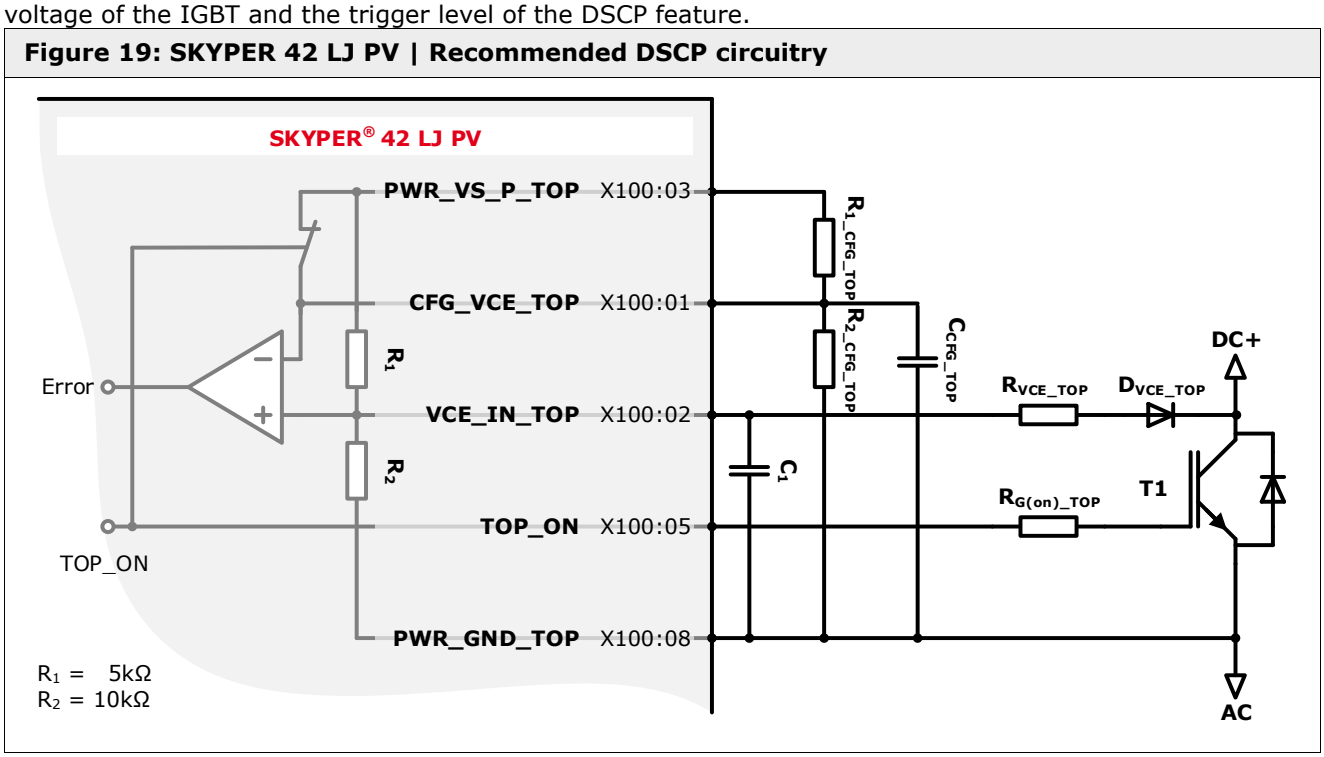
5.5 Dynamic short circuit protection by V_{CEsat}-monitoring (DSCP)

The dynamic short circuit protection feature monitors the Collector-Emitter voltage V_{CE} of the semiconductor during on-state. When the feature is enabled and the voltage at the *VCE_IN* input exceeds the voltage reference level at the *CFG_VCE* input the driver will enter into an error state and will execute its error routine as described in chapter 5.1.
The DSCP feature can be disabled by connecting the *CFG_VCE* pin to the *PWR_VS_P* pin and the *VCE_IN* pin to the *PWR_GND* pin.

Important note

The DSCP feature is designed to detect short circuit conditions and forces the driver to react on a desaturation event of a semiconductor. It is explicitly stated that this function is designed to detect short circuit conditions and not to set a specific threshold to detect overcurrent situations e.g. of externally connected applications. It is recommended to set the DSCP trip level to a value of 7V to 9V (voltage at the *CFG_VCE* pin) to prevent from unwanted accidently (false) triggered desaturation events due to a too small gap between the saturation voltage of the IGBT and the trigger level of the DSCP feature.

Figure 19: SKYPER 42 LJ PV | Recommended DSCP circuitry



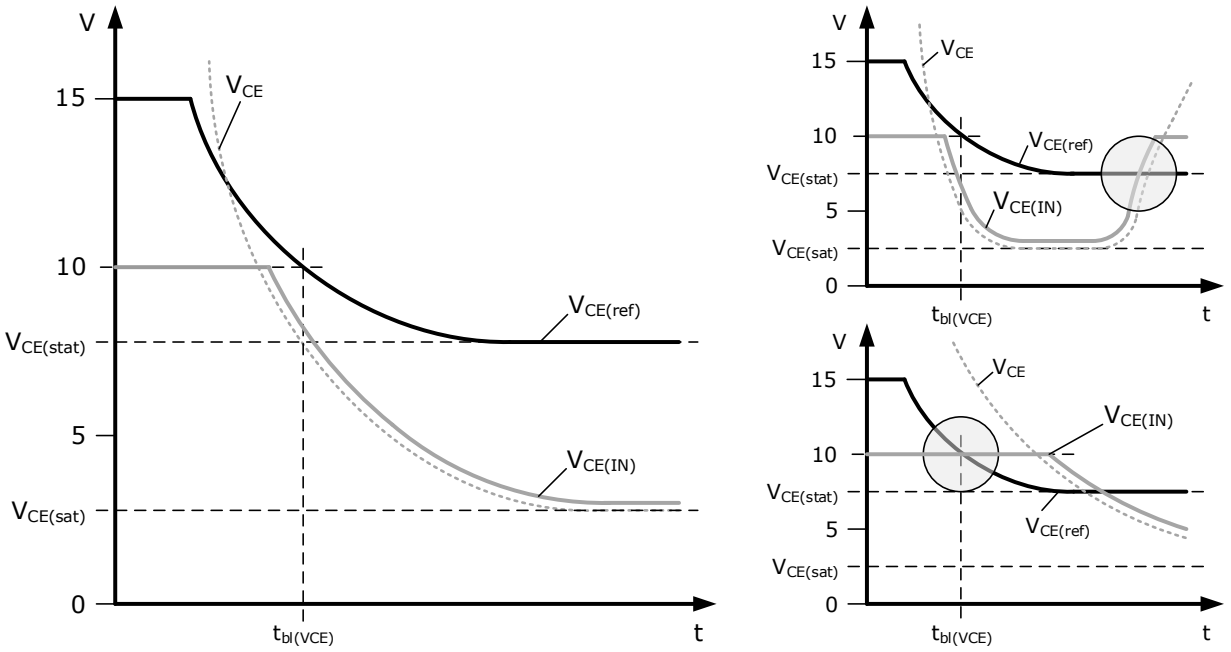
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Recommended values		
Component	**Value**	**Remark**
C_1	≤1nF	Optional filter capacitors suppressing high-frequency interfering signals.
C_{CFG}	-	Dimensioning according to chapter 5.5.2
D_{VCE}	-	- The diode must block V_{CEmax}, when the IGBT switches off - The diode must provide functional insulation - Revers recovery charge of the diode causes additional pulse loads at R_{VCE}
R_{1_CFG}	~30kΩ	Dimensioning according to chapter 5.5.2
R_{2_CFG}	-	Dimensioning according to chapter 5.5.2
$R_{G(on)}$	-	Dimensioning according to chapter 4.10
R_{VCE}	511Ω	Resistor should be surge proof

5.5.1 DSCP | Functional description

If the driver keeps the connected semiconductor in off-state the high voltage diode D_{VCE} is operating in reverse direction. The voltage $V_{CE(IN)}$ at the *VCE_IN* pin is set to 10V by the voltage divider of R_1 and R_2. The *CFG_VCE* pin is internally shorten to *PWR_VS_P* and pulls the voltage $V_{CE(ref)}$ at the *CFG_VCE* pin to *PWR_VS_P*. Hence, the output of the internal comparator is forced to its negative rail voltage.
When the driver initiates the turn-on process of the semiconductor the internal bypass will be interrupted and the capacitor C_{CFG} discharges until the voltage level, defined by the voltage divider of R_{1_CFG} and R_{2_CFG}, is reached. The trip level during the on-state of the semiconductor has reached its static level ($V_{CE(ref)}$ = $V_{CE(stat)}$).
Simultaneously to the discharging process of the capacitor C_{CFG} the semiconductor starts conducting and reducing the Collector-Emitter voltage V_{CE} to V_{CEsat}. When the Collector-Emitter voltage of the IGBT falls below 10V the high-voltage diode D_{VCE} is starting to operate in forward direction. Now, the voltage $V_{CE(IN)}$ at the *VCE_IN* pin follows the Collector-Emitter voltage of the semiconductor with an offset caused by the forward current I_F of the high-voltage diode D_{VCE} multiplied by the resistance of R_{VCE} plus the voltage drop V_F of the high-voltage diode.
The DSCP feature is active from the moment the voltage $V_{CE(ref)}$ at the *CFG_VCE* pin is below 10V. The time elapsed from initiating the turn-on process of the semiconductor until the DSCP feature is activated is called blanking time $t_{bl(VCE)}$.
In active state the DSCP triggers an error event, if the voltage $V_{CE(IN)}$ at the *VCE_IN* pin exceeds the voltage $V_{CE(ref)}$ of the *CFG_VCE* pin.
Figure 20 shows on the left side the above described process for a well-configured blanking time $t_{bl(VCE)}$ and static threshold voltage $V_{CE(stat)}$.
The upper right side of Figure 20 shows a desaturation event of an IGBT during the DSCP feature is active. In the moment when the voltage $V_{CE(IN)}$ exceeds the threshold voltage $V_{CE(ref)}$ the driver enters into error state. The lower right side shows an error condition caused by a too short determined blanking time $t_{bl(VCE)}$. The threshold voltage $V_{CE(ref)}$ has already fallen below 10V before the monitored voltage $V_{CE(IN)}$ is below that level.

Figure 20: SKYPER 42 LJ PV | Dynamic short circuit protection



5.5.2 DSCP | Calculation hints

The following equations help to select all relevant parameters of the DSCP feature:

Equation (1) Calculation of the static trip level $(V_{CE(ref)} = V_{CE(stat)})$

$$V_{CE(stat)} = PWR_{VS_P} \cdot \frac{R_{2_{CFG}}}{R_{1_{CFG}} + R_{2_{CFG}}}$$

Equation (2) Calculation of R_{2_CFG} for a certain value of $V_{CE(stat)}$

$$R_{2_CFG} = \frac{R_{1_CFG} \cdot V_{CE(stat)}}{PWR_VS_P - V_{CE(stat)}}$$

Equation (3) Calculation of the blanking time $t_{bl(VCE)}$ depending on the values of C_{CFG}; R_{1_CFG}; R_{2_CFG}; $V_{CE(stat)}$

$$t_{bl(VCE)} = -C_{CFG} \cdot \frac{R_{1_{CFG}} \cdot R_{2_{CFG}}}{R_{1_{CFG}} + R_{2_{CFG}}} \cdot \ln\left(\frac{\frac{10V}{PWR_{VS_P}} \cdot \left(R_{1_{CFG}} + R_{2_{CFG}}\right) - R_{2_{CFG}}}{R_{1_{CFG}}}\right)$$

Equation (4) Calculation of the voltage $V_{CE(IN)}$ at the *VCE_IN* input depending on the values of V_{CE}; R_{VCE}; $V_{D_{VCE}}$

$$V_{CE(IN)} = \frac{R_1 \cdot R_2}{R_1 \cdot R_2 + (R_1 + R_2) \cdot R_{VCE}} \cdot V_{CE} + \frac{\left(V_{D_{VCE}} + \frac{PWR_{VS_P} \cdot R_{VCE}}{R_1}\right) \cdot R_1 \cdot R_2}{R_1 \cdot R_2 + (R_1 + R_2) \cdot R_{VCE}}$$

5.6 Active clamping

The driver offers the possibility to reduce over voltages during the turn-off event of the IGBT by using an active clamping feature. Figure 22 shows an example of an active clamping circuitry based on Zener diodes. The total breakdown voltage of the Zener diodes D_{CLMP} determine the voltage level when the clamping starts. If the collector-gate voltage V_{CG} rises beyond the break down voltage V_{Zener} during a turn-off of the IGBT, the clamping diodes will conduct. This leads to a current feeding energy into the gate of the IGBT and gradually switches the IGBT on again until the V_{CG} voltage is reduced below the V_{Zener} reference.
If the voltage at the input exceeds the threshold of 13V, the *CLMP_IN* input indicates to the driver that the collector-gate voltage has risen above V_{zener}. When entering active clamping mode the driver sets the output channels to high impedance, which reduces the losses on the driver.

Figure 21: SKYPER 42 LJ PV | Active clamping

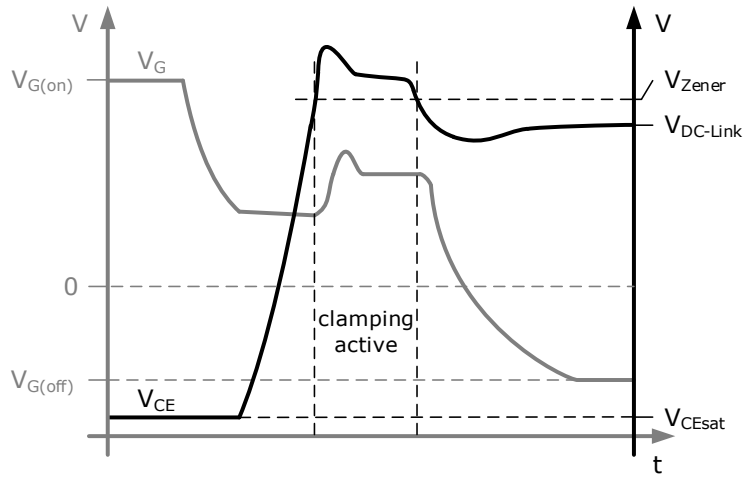
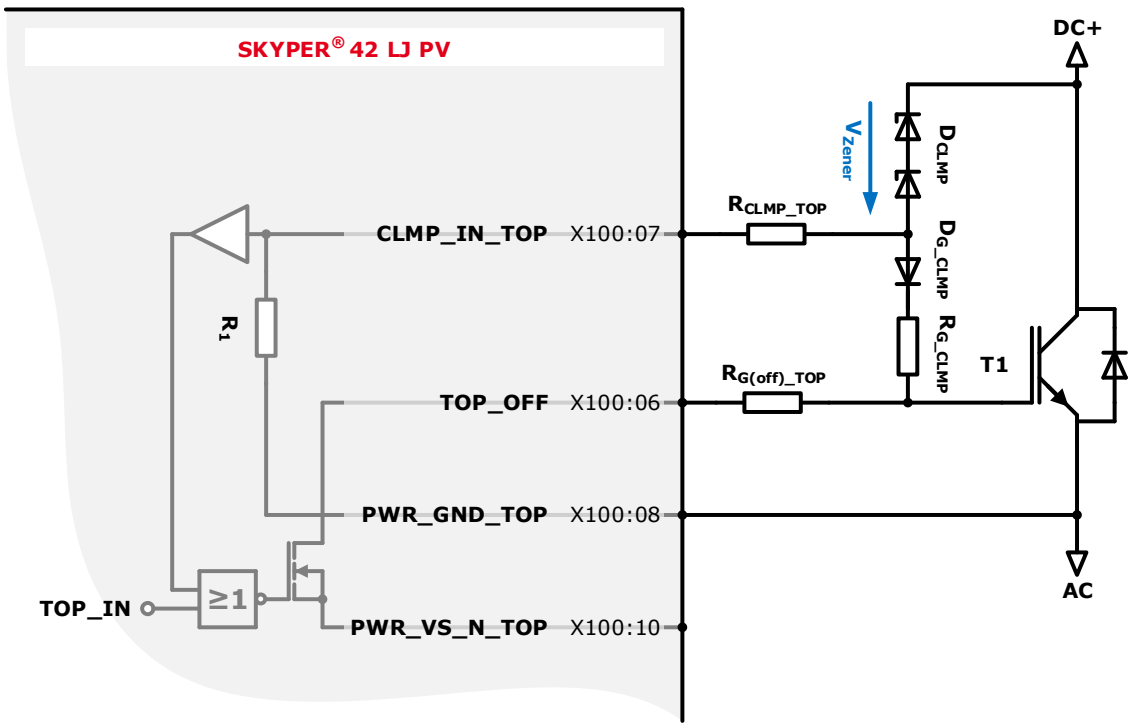


Figure 22: SKYPER 42 LJ PV | Application example for active clamping



Important Note

During the clamping process the IGBT is operating in the linear mode, which is typically not specified. The suitability of the power semiconductor to operate under such linear conditions and the risk of creating oscillations, and therefore potentially creating considerable additional losses, must be considered and verified. In any case, active clamping must not be operated during standard switching to avoid thermal overstress and reduced IGBT lifetime.

Parameter	**Min**	**Typ**	**Max**
Threshold high CLMP-input	-	-	13 V
Threshold low CLMP-input	2 V	-	-

5.7 Soft Off

The SKYPER 42 LJ PV provides a separate turn-off path *TOP_SOFTOFF/BOT_SOFTOFF* activated by the driver, if an error event is detected on the secondary side, as described in chapter 5.1. Switching-off a semiconductor via the soft-off path aims to reduce the switching speed of the semiconductor and, hence, the over voltage caused by the di/dt through the system's stray inductances is decreased.

Recommendation
Usually the Soft Off resistor is roughly 10 times as high as the standard $R_{G(off)}$. However, the proper value must be very carefully evaluated in the system in accordance with the individual application parameters. The setup is a balance between staying within the maximum permitted short circuit time of the IGBT and on the other hand to reduce the overvoltage below the maximum Collector-Emitter voltage of the IGBT. Please observe the individual SCSOA of your power semiconductor.

5.8 Safe short circuit turn-off in multilevel topology

Power semiconductors in multilevel NPC applications need careful control, especially in error conditions like a short circuit. A dedicated 3-L topology turn-off sequence avoids damaging the semiconductors due to an unappropriated turn-off sequence. The integrated DSCP, Soft Off, and active clamping features ensure that the SKYPER 42 LJ PV allows proper control of the power semiconductors in multilevel applications. Thanks to the advanced error management provisions realized in the ASIC chipset the SKYPER 42 LJ PV safely handles even short circuit conditions.

Detailed information how to use the SKYPER 42 LJ PV driver core in multilevel applications can be found in the Application Note AN_19-001 rev.00 "Gate Driver Configuration and Short Circuit Protection for 3-Level Topologies". Thoroughly reading this document is highly recommended before starting tests of multilevel topologies.

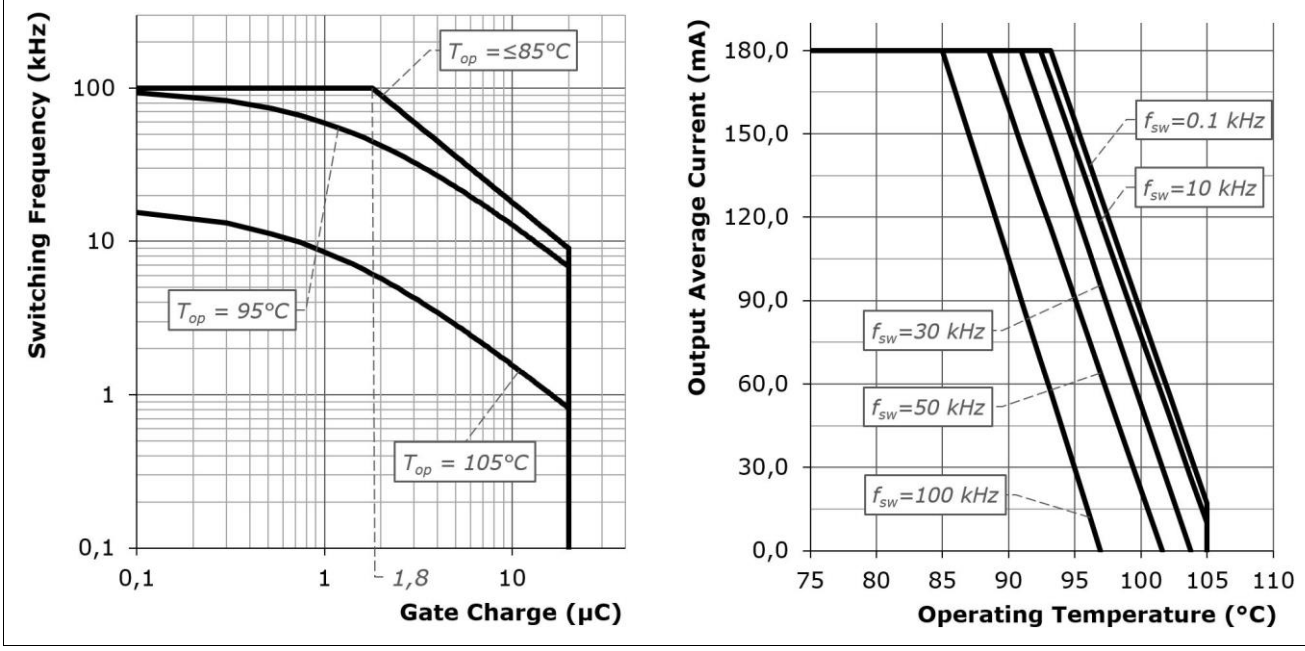
6. Electrical Characteristic

The performance of an IGBT driver is conditional on the operating temperature and the gate charge of the IGBT that it drives. The gate charge of an IGBT is, in general, dependent on the IGBT generation and its specific construction. Furthermore, it has a variable value which is depending on various parameters, mainly the chip size, the Collector-Emitter voltage V_{CE}, and the Gate-Emitter voltage V_{GE} that is supplied by the driver. The datasheet of a module usually provides the gate charge value as a function of the applied Gate–Emitter voltage V_{GE} for a defined constant Collector-Emitter voltage V_{CE}.

The SKYPER 42 LJ PV driver core performs at a maximum switching frequency of 100 kHz under operating temperature up to 85°C and gate charge up to 1.8 µC on each output. It is approved for an operating temperature up to 105°C and 20 µC loads. As indicated on the left-hand side of Figure 23, the maximum allowable applied switching frequency is derated with the gate charge of the connected IGBT. However, it is recommended to use external boost capacitors to maintain the stability of the gate drive voltages $V_{G(on)}$ and $V_{G(off)}$ for gate charge ≥2.5 µC as described in 4.11. Please refer to Figure 23 below for the derating of the SKYPER 42 LJ PV under various operating points.

For operations with gate charge larger than 20 µC, please contact our sales team for further support.

Figure 23: SKYPER 42 LJ PV | Derating Charts



7. Product Qualification

Table 9: SKYPER 42 LJ PV | Routine tests			
test	**test category**	**test description**	**Standard**
AOI	Automated Opt. Inspection	Control of accurate placement of components/ of solder joints, 100%	Semikron Danfoss
ICT	In-Circuit Test	Test of the populated PCB, checking the correctly fabrication, 100%	Semikron Danfoss
FAT	Function Test	Supply current, gate on/off, UVP, error, 100%	Semikron Danfoss

Table 10: SKYPER 42 LJ PV | Approval tests			
test	**test category**	**test description[1]**	**Standard**
EP	Electrical Parameters	ϑamb = -40°C / +105°C	Semikron Danfoss
ST	STEP Test	20x 10µs to 2s interruption	IEC 61000-4-29
ISO	Isolation	5.0 kV AC rms, 60s	IEC 50178
TC	Thermal Cycling	500 cycles a 1h, -50°C – 105°C	IEC 60068-2-14
TH	Temperature Humidity	85°C, 85% RH, 1000h	IEC 60068-2-67
BST	Burst	Power terminals: 4kV; Control terminals: 4kV	IEC 61000-4-4
HT	High Temp Operation	95°C, 500h	SEMIKRON
ESD	ESD	Contact discharge: 6kV; Air discharge: 8kV	IEC 61000-4-2
RFF	Radio Frequency	80 MHz – 2.7GHz, 30 V/m, 80% AM 1kHz	IEC 61000-4-3
RFD	RF Conducted Disturbance	150 kHz - 80 MHz, 20 V/m, v+h, 80 % AM 1kHz	ICE 61000-4-6
VB	Vibration[2]	**Sinusoidal** 20Hz to 500Hz, 5g 26 Sweeps per axis (x, y, z) **Random** 10Hz to 2000Hz, 3g, 2h per axis (x, y, z)	IEC 60068-2-6
SH	Shock[2]	Half-sine pulse, 30g, 6000 shocks, 18ms, 6 axis (±x, ± y, ± z)	IEC 60068-2-27

[1] The test conditions are not the maximum applicable conditions for the products. The characteristics of the products are indicated in the data sheet
[2] Please see Chapter 3.2. for more details

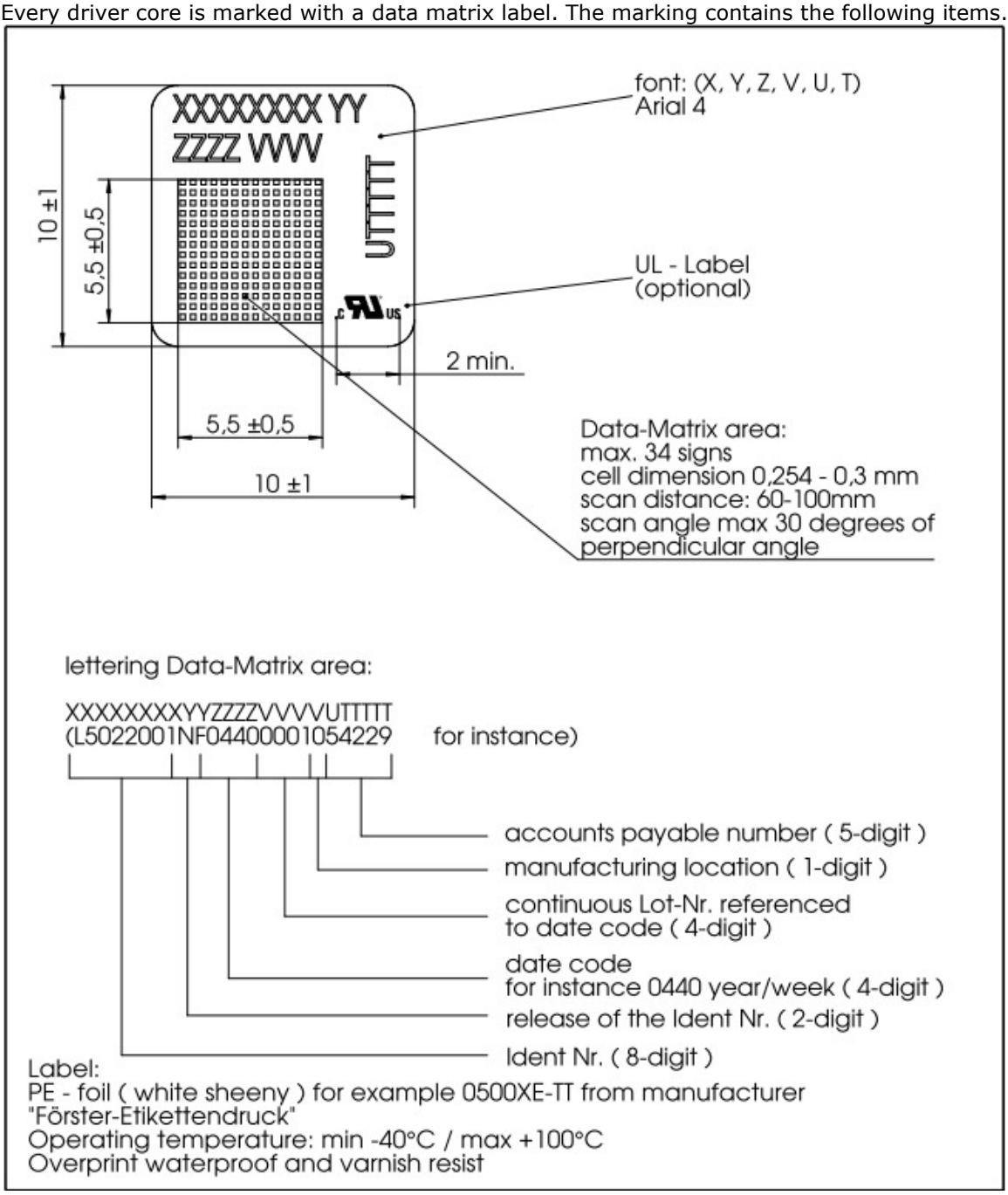
8. Environmental conditions

Table 11: SKYPER 42 LJ PV | Environmental conditions		
Insulation parameters	**Rating**	**Norm / Standard**
Grid voltage	690V	IEC 50178
Pollution Degree	PD II	IEC 50178
Maximum altitude	2000 meter above sea	IEC 50178
Overvoltage category	OVC III	IEC 50178
Isolation resistance test, primary to secondary side (2 pieces per lot as series test, power and signal transformers are 100% tested as series test)	5000 V AC rms, 60s	IEC 50178
Rated insulation voltage	12 kV Cat. III	IEC 60664-1
Creepage/clearance distance, primary/secondary side	≥15.1mm	IEC 50178
Creepage/clearance distance, secondary/secondary side	≥7.6mm	IEC 50178
Climate	**Rating**	**Norm / Standard**
Climate class	3K3	IEC 60721-3-3
Environmental conditions	**Rating**	**Norm / Standard**
Operating temperature	-40... +105 °C	
Storage temperature	-40... +85 °C	
Flammability	Heavy flammable materials only	UL94 V0
		RoHS / WEEE / China RoHS
EMC Condition	**Rating**	**Norm / Standard**
ESD	6 kV contact discharge / 8 kV air discharge	IEC 61000-4-2 IEC 61800-3
Burst	≥ 2kV on adaptor board for signal lines	IEC 61000-4-4 IEC 61800-3
Immunity against external interference	≥ 30V/m 80MHz – 2700 MHz	IEC 61000-4-3 IEC 61800-3
Immunity against conducted interference	≥ 20V 150kHz – 80MHz	IEC 61000-4-6 IEC 61800-3
Shock Vibration	**Rating**	**Norm / Standard**
Vibration	**Sinusoida**l 20Hz … 500Hz, 5g, 26 sweeps per axis (x, y, z) **Random** 10Hz … 2000Hz, 3g 2 h per axis (x, y, z)	IEC 60068-2-6
Shock	6000 Shocks (6 axis: +-x, +-y, +-z, 1000 shocks per axis), 30g, 18ms (The connection between driver and PCB was reinforced by a support post during the test.)	IEC 60068-2-27

9. Marking

Figure 24: SKYPER 42 LJ PV | Label

Every driver core is marked with a data matrix label. The marking contains the following items.



10. Change history

Revision	Date	Changes
00	2020-09-28	Initial version
01	2020-10-28	“Chapter 6 Electrical Characteristic” added
02	2024-02-07	Configuration pins primary side connection hints added. Template update.

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References

[1] www.semikron-danfoss.com
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, “Application Manual Power Semiconductors”, 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3

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